THE DESIGN AND FABRICATION OF A SIMPLIFIED BISTATIC RADAR PROCESSOR

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THESIS

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December 1972

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Submitted in partial fulfillment of the
requirements for the degree of

ELECTRICAL ENGINEER

from the

NAVAL POSTGRADUATE SCHOOL
December 1972

ABSTRACT

Bistatic radar is different from conventional (monostatic) radar in that the transmitting and receiving antennas are in separate locations. For purposes of this thesis the transmitting radar will be assumed to be located up to 100 miles from the bistatic radar receiver. It will have a circular scan antenna with a constant rotation rate. The plan position indicator (PPI) display of the video from the bistatic radar receiver has both angular and range distortion caused by the wide separation of the transmitting and receiving antennas.

The bistatic radar processor receives video signals from the bistatic receiver and processes them to obtain the information required to synchronize the PPI display's rotation in rate and phase to the rotation of the transmitting antenna and to correct the range errors.

This thesis discusses the design and fabrication of a simplified version of the processor and how it accomplishes the functions mentioned above.

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ACKNOWLEDGEMENT

The author would like to thank the personnel at Naval Avionics Facility, Indianapolis (NAFI), who provided the outstanding support, both material and technical, which made it possible to design and build this simplified bistatic radar processor during a two month period at NAFI. Mr. David S. Ferguson, of NAFI, who introduced the author to integrated circuit design and supplied much needed instruction and guidance in the design of the processor deserves a special vote of thanks. Without his expertise and the willingness with which he diverted his time from his many other projects the processor would never have been completed in the time available.

The author's thesis advisor, Professor David. B. Hoisington, also receives the author's heartfelt thanks for the numerous rough drafts which he read and his very helpful recommendations for revision and clarification.

I. INTRODUCTION

In most radar systems a common antenna is used for both transmitting and receiving. Such a radar is a monostatic radar, and is the most common type of radar system in use today. However, another less common system called bistatic radar is well known. In this system, the transmitting and receiving antennas may be widely separated.

The separation of the transmitting and receiving antenna locations in bistatic radar results in widely divergent radar characteristics from those associated with monostatic radar. If a scanning transmitting antenna is assumed with an omnidirectional receiving antenna, as is the case throughout this treatise, range and angular errors are introduced which are not present in monostatic radar.

A. ANGULAR ERROR AND ITS CORRECTION

Angular error is produced if a sweep of the plan position indicator (PPI) display at the receiver is not rotating at the same rotation rate or is not in phase with the rotation of the transmitting antenna. To keep the rotational speed of the PPI equal to the antenna rotational speed, an automatic speed-control circuit was incorporated in the bistatic radar processor. This circuit operates by detecting the times at which the main lobe of a radar is illuminating the bistatic radar receiver. A voltage proportional to the time between successive illuminations is generated and used to

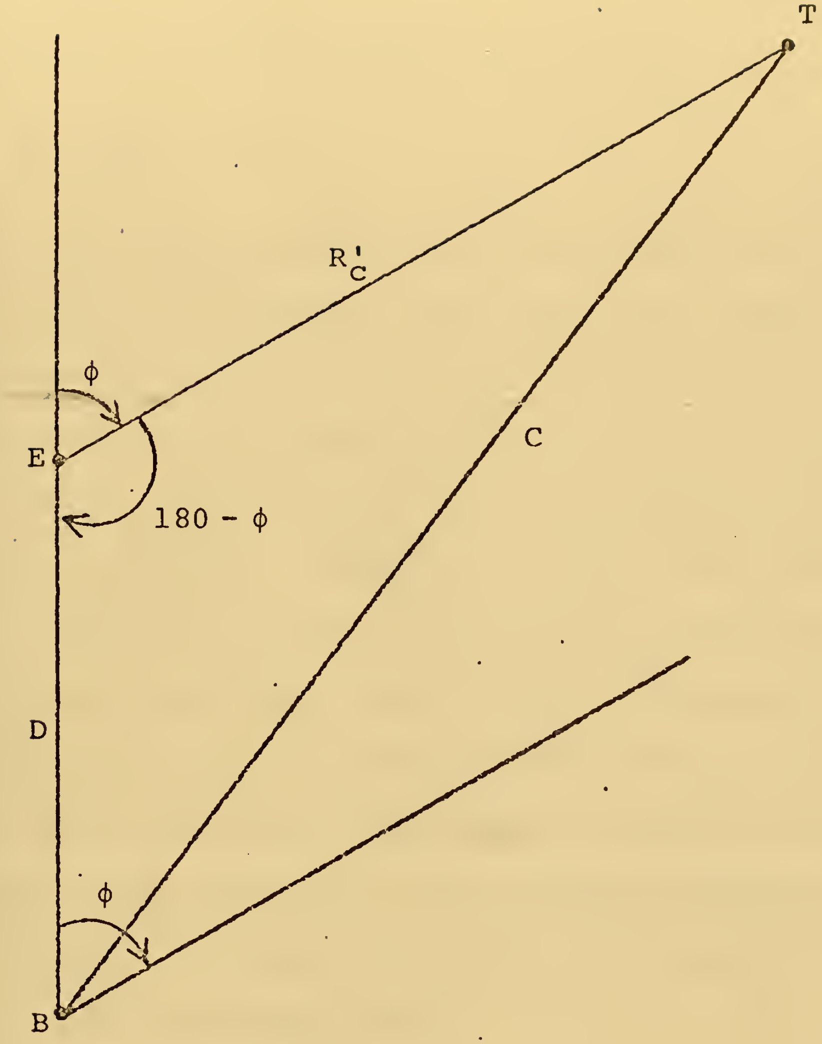
adjust the speed of the PPI DC drive motor to the same speed as the transmitting antennas.

With the PPI sweep and the transmitting antenna rotating at the same speed, the phase error must be eliminated so that they are both pointing in the same direction at the same time. The decision was made to set the system up so that when the transmitting antenna is looking at the bistatic receiver the PPI sweep is pointing at 180 degrees relative to the face of the display unit. A feather pulse is generated and displayed on the PPI each time the receiver is illuminated by the transmitting antenna. The phase error is eliminated by circuitry which temporarily speeds the motor up or slows it down until the feather occurs at 180 degrees, and then readjusts the motor speed to coincide with the antenna rotation rate of the transmitter. Now, as long as the feather occurs on the PPI at 180 degrees on every sweep there is no doubt that the PPI sweep is synchronized in rotation rate and phase with the transmitting antenna.

B. RANGE ERROR AND ITS CORRECTION

The range error problem is best understood by reference to Fig. 1 in conjunction with the following discussion.

In monostatic radar the true range R_c', from E to T, would be computed by transmitting a radar pulse and measuring the time it took to travel from E to T and back. But, in bistatic radar, if the signal propagated from the radar to the target and back to the radar in a time equal to the difference between the signal transit time from the radar to target to



E - Radar emitter location

B - Bistatic radar receiver location

T - Target location

R'_c - Correct range

R_a - Apparent two way range

D - Distance between emitter and receiver

C - Distance between target and receiver

ϕ - Angle between extended line of sight from B to E and line of sight from E to T

Figure 1. Bistatic Radar Geometry.

bistatic receiver and the transit time from radar to bistatic receiver, the range would be given by

$$R_a = R_c' + C - D. \qquad (1)$$

This is called the apparent range, and equals the correct range R_c' only in the special case where the target, radar and bistatic receiver lie on a line with the radar between the other two. In equation (1), R_c', C and D are the lengths of the indicated paths while R_a is the distance from radar to a target and back. Therefore, R_a will be called a two-way range while R_c', C and D will be called one-way ranges.

In order to find the actual range from radar emitter to target from the data available at the bistatic receiver site, one must assume he knows the distance D between the transmitting and receiving sites. The unknown distance C can be calculated from the geometry of Fig. 1 by using the law of cosines. This gives the result

$$C^2 = R_c'^2 + D^2 + 2R_c D \cos \phi. \qquad (2)$$

Equation (1) can be solved for C and substituted into equation (2). Solving the resulting equation for R_c' gives

$$R_c' = \frac{R_a^2 + 2R_a D}{2R_a + 2D(1 + \cos \phi)} . \qquad (3)$$

In this equation R_c' is a one-way range. In order to convert it to a two-way range one simply multiplies by two giving

$$R_c = \frac{R_a^2 + 2R_aD}{R_a + D(1 + \cos \phi)}, \tag{4}$$

the desired result.

This is the form of the bistatic radar range equation which has been used in former electronic implementations of range correction. However, Navy LCDR Ralph D. Hudson suggested the following simplification in a personal communication to Mr. David S. Ferguson of Naval Avionics Facility, Indianapolis. If the substitution $\cos \phi = \frac{y}{R_c}$ is made in the equation for R_c the result is

$$R_aR_c + DR_c + Dy = R_a^2 + 2R_aD. \tag{5}$$

Solving for R_c yields

$$R_c = \frac{R_a^2 + 2R_aD - Dy}{R_a + D} = \frac{R_a(R_a + D) + D(R_a - y)}{R_a + D}$$

$$= R_a + \frac{D(R_a - y)}{R_a + D}. \tag{6}$$

Electronic implementation of this form of the range equation is considerably less complicated. It takes fewer components and is less costly.

The range correction circuit for the bistatic radar processor was designed to provide range correction only on the 50 mile range scale. Extending correction to the other range scales would require some switching logic and a set of input resistors for each range scale. It was felt by the

author that the additional time required to design and construct this circuit was not indicated because the effort would simply be repetitious.

II. BACKGROUND

The author spent a two month period at Naval Avionics Facility, Indianapolis (hereafter abbreviated as NAFI) designing and fabricating the simplified bistatic radar processor discussed in this treatise. This work was done under the guidance of Mr. David S. Ferguson.

A. STANDARD HARDWARE PROGRAM

Because of its availability at NAFI, Standard Hardware Program (SHP) packaging was used throughout the system. SHP is an electronic module standardization program coordinated throughout the Navy by the Naval Electronic Systems Command.

The basic building block in SHP is the module shown in Fig. 2. This module is 2.62 inches in length, 1.95 inches in height and 0.29 inches in thickness. It has provision for a printed circuit (PC) board to be glued to each side. There are twenty contacts available to each PC board for input/output connections. The 40 contacts are extended through the bottom of the module where they emerge as male connector pins.

The modules are mounted in a card cage with slots for the flanges to slide into on each end of the module. The connectors on the bottom of the module mate with female connectors on the bottom plate of the card cage. This bottom plate is called a wirewrap plate because its female

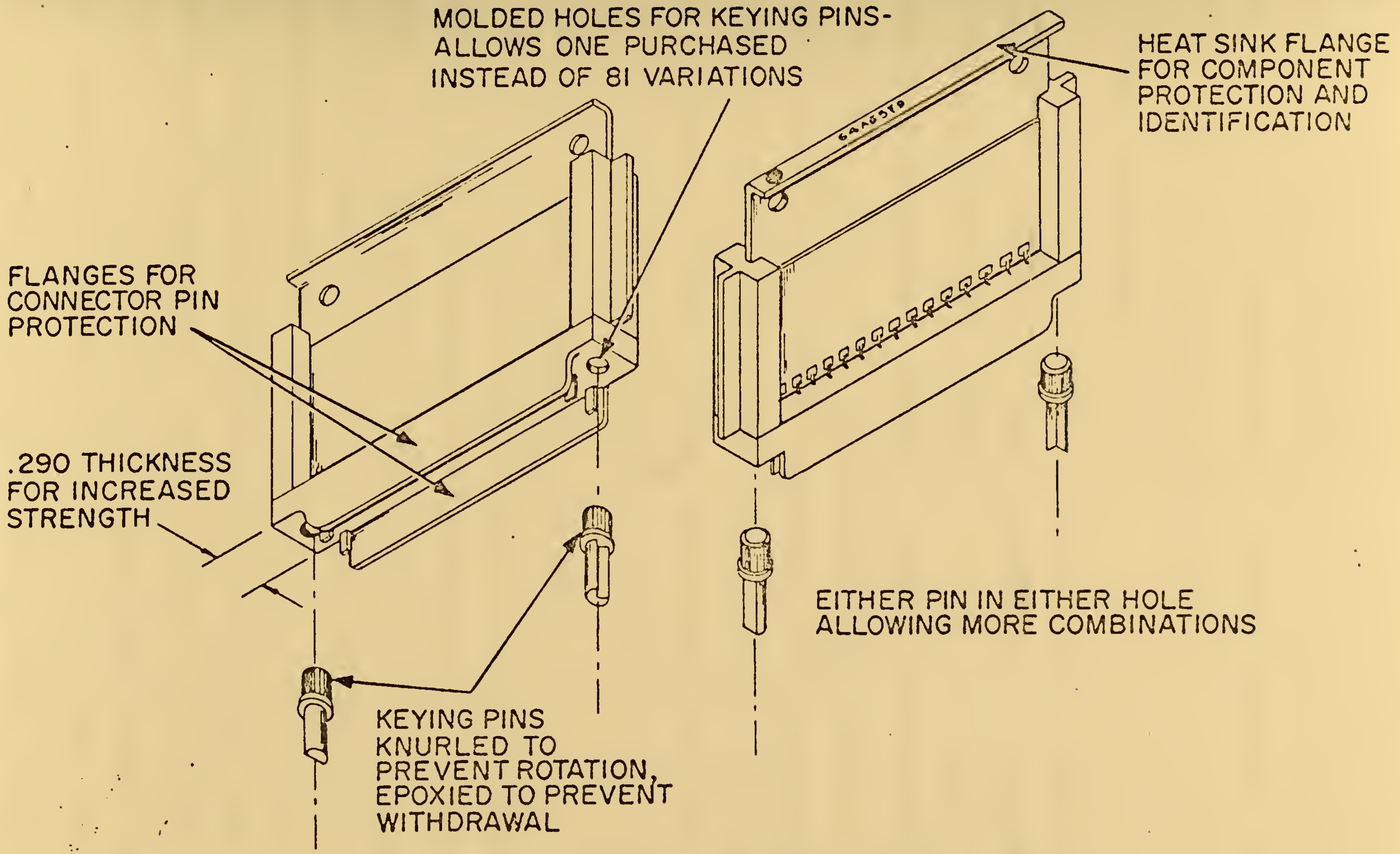


Figure 2. Standard Hardware Module.

connectors emerge on the bottom as long male connector pins to which connections are made by wrapping wire around them very tightly with a special tool. Figure 3 shows the layout for the card cage used in the processor.

B. EXTERNAL EQUIPMENT

The bistatic radar processor cannot function usefully by itself. It requires a radar receiver with its associated antenna system and a PPI display unit. The PPI display unit utilized in the present system is a Hewlett Packard 1300A X-Y display. In order for the display to be useful as a PPI it must have P3 or at least P7 phosphor. Less persistent phosphors will not retain luminescence for the period necessary to display a radar picture. The HP-1300A requires X, Y and -Z inputs from the processor.

C. METHOD OF DRIVING SWEEP OF X-Y DISPLAY

The sweep of the X-Y display must be rotated in synchronization with the antenna rotation rate of the transmitting antenna. The two options available were to drive the sweep electronically or with a DC motor. The electronic option was eliminated because of the complexity, cost, time available for design and construction, and the fact that NAFI already had an operational system utilizing that method. By contrast, the DC motor option was much less complex and more likely to be completed in the time frame available. It had the added attraction of being a first-attempt design rather than a rehash of a previously designed circuit.

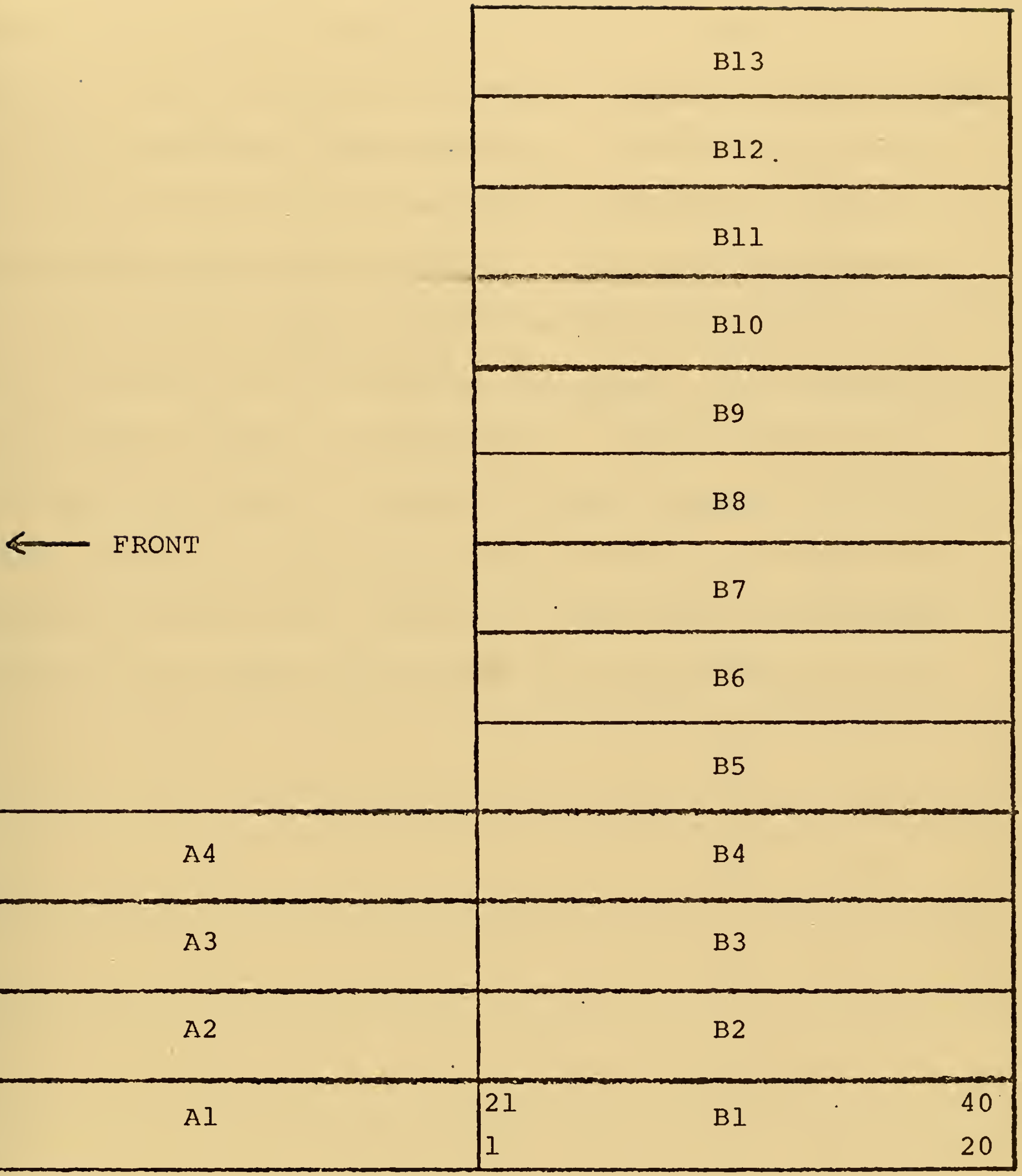


Figure 3. Card Cage Layout (top view).

D. BUILT-IN-TEST SIGNAL GENERATOR

Due to the difficulty in obtaining the required test signals from standard signal generators to check out the processor it was necessary to design a built-in-test system. This system generates approximately a 500 PPS sync signal with a burst of several pulses of the same PRF occurring approximately every eight seconds. The signal simulates a radar with a PRF of 500 PPS whose antenna rotation is at a period of eight SPR (seconds per rotation). This signal is used to check out the entire system. The only thing not available is an input to present a video picture on the PPI display. However, the video summing circuit can still be checked out because the intensity, range marks and feather signals are available for summing and presentation on the PPI.

III. THEORY OF OPERATION

The bistatic radar processor system has been divided into six functional groups or subsystems. These subsystems and their interconnections are shown in Fig. 4.

The system requires two inputs from a radar receiver. They are a video signal and a feather signal. The video signal is split and fed into the system at the video input connector which leads to the output circuit and at the sync, or trigger, input which leads to the sweep generator circuit. The feather signal is tapped out of the receiver just after the tuner. It is such a low level signal that a detector at this point should only produce an output when the main lobe of the radar is illuminating the receiver antenna. This signal is amplified with a video amplifier and fed into the system at the feather input which leads to the feather circuit. The sync and feather inputs may be obtained from the built-in-test signal generator by throwing a DPDT switch on the back panel of the processor.

The sweep-generator circuit generates a linear ramp voltage which is utilized by the output circuit to provide X and Y output voltages which drive the X and Y deflection plates of the X-Y display to give a PPI presentation. It generates range marks which are fed through the output circuit to produce range rings on the PPI. It also provides a logic signal to the feather circuit.

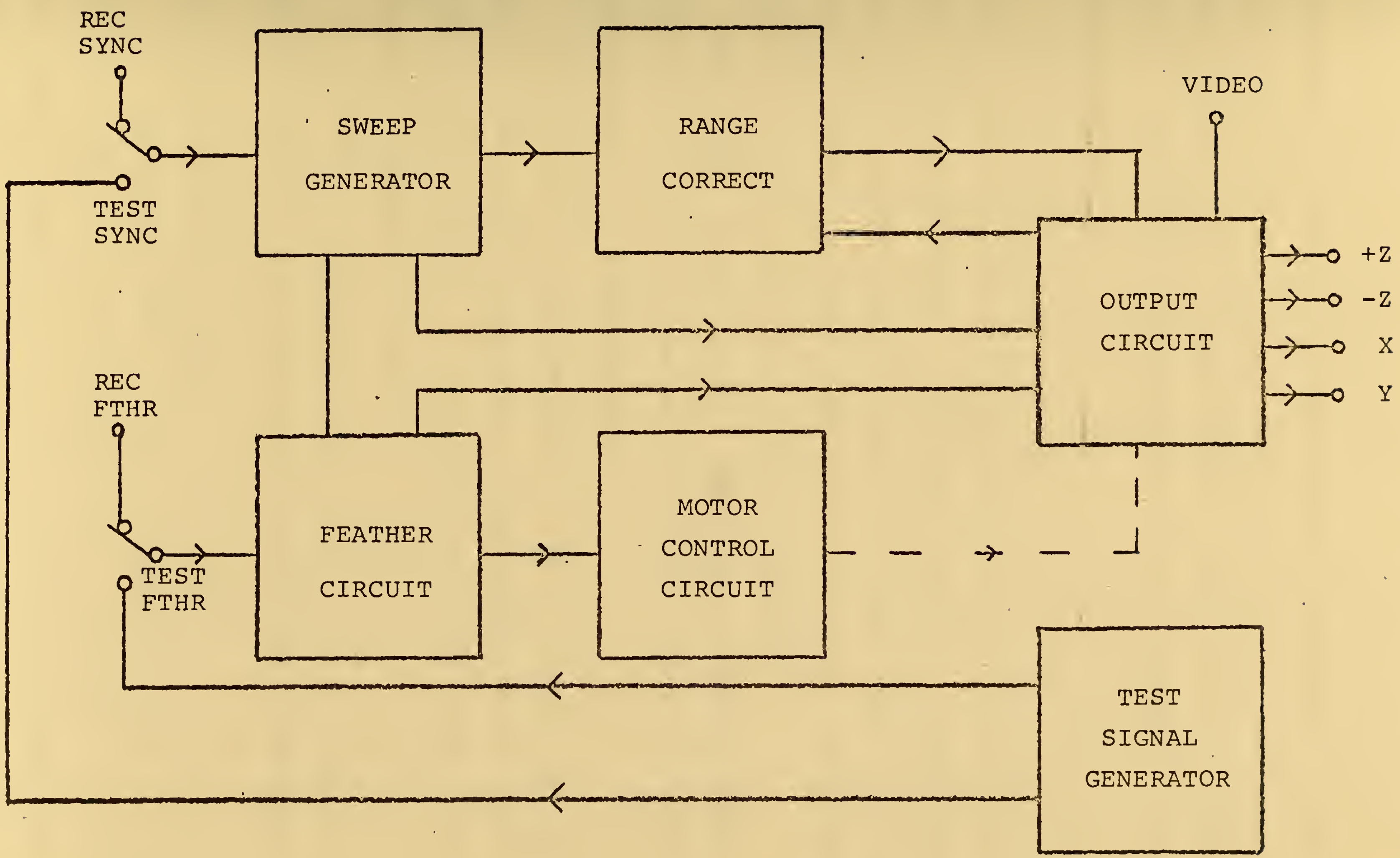


Figure 4. System Block Diagram.

The range-correction circuit accepts the linear ramp voltage from the sweep generator and adds a non-linear correction voltage to compensate for the bistatic radar range error. It then feeds the corrected, and now non-linear, ramp voltage to the output circuit where it can be selected for use instead of the uncorrected ramp voltage by throwing a DPDT switch.

The feather circuit produces both a video and a logic signal each time the bistatic receiver is illuminated by the main lobe of the radar. The video signal is passed through the output circuit and appears as a bright spike or feather of video eminating from the center of the PPI. The logic signal is fed to the motor control circuit.

The motor control circuit generates a voltage which synchronizes the motor with the rotation rate and phase of the transmitting radar antenna.

The output circuit contains a video summing amplifier to sum all the signals which are to be displayed on the PPI, and it also provides the voltages which drive the X and Y deflection plates of the PPI.

Each of the subsystems shown in Fig. 4 is broken down and discussed in more detail in the following paragraphs.

A. SWEEP GENERATOR CIRCUIT

The sweep generator circuit, as shown in Fig. 5, functions in the following manner. A trigger signal, video from the bistatic receiver, is fed in through the sync input to the threshold detector. Those pulses which exceed the

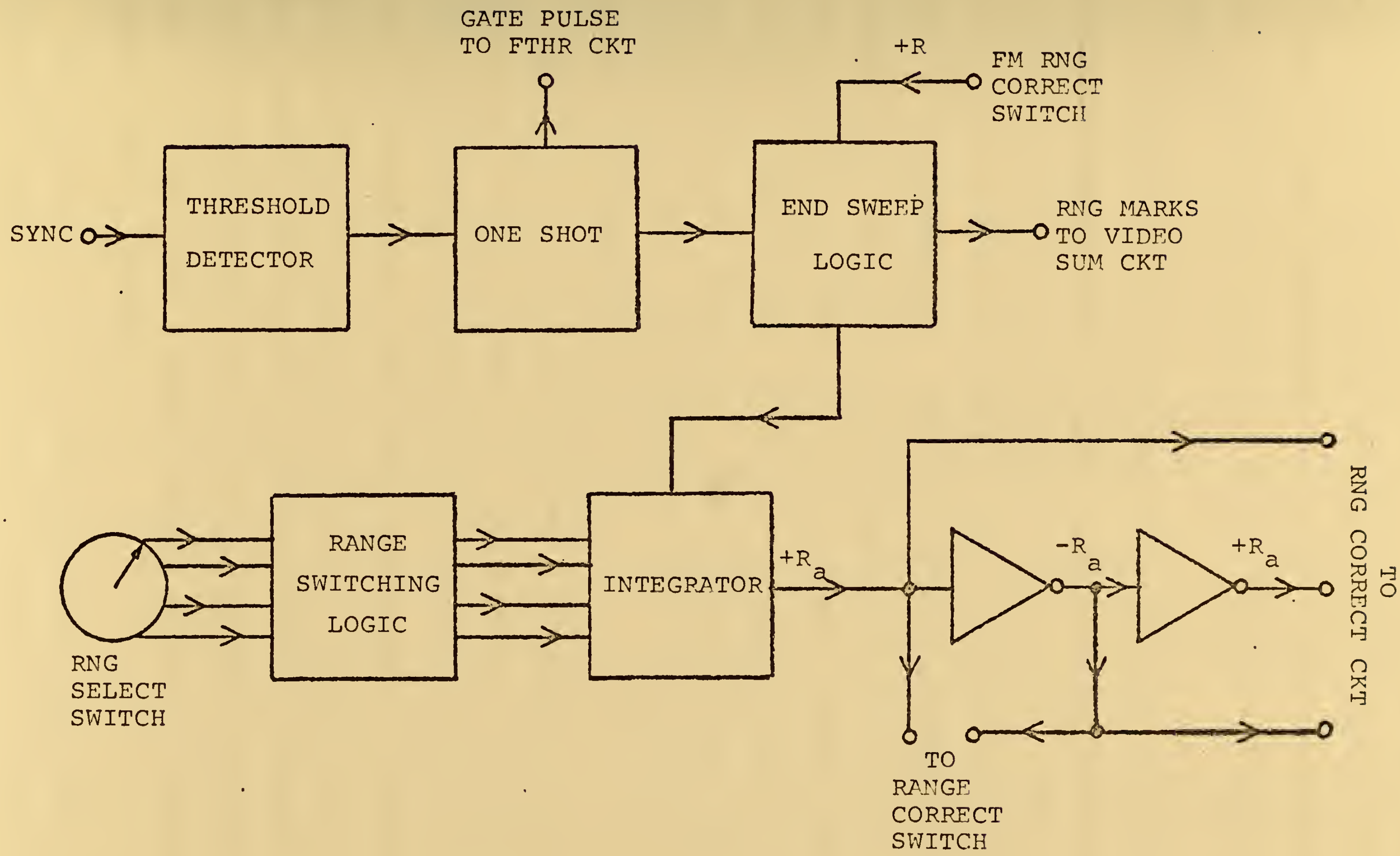


Figure 5. Sweep Generator Circuit.

threshold level established with the threshold set potentiometer on the front panel produce a logical one at the output of the threshold detector. The threshold should be set so that target returns and noise cannot trigger the threshold detector.

A logical one to the one-shot module produces a one-microsecond gating pulse to the feather circuit and a 360-microsecond pulse to the end-sweep-logic module. The pulse to the end-sweep-logic module produces a logic level which turns the integrator on. The integrator generates the sweep voltage $+R_a$, a positive linear ramp, which is fed to the range correction circuit, the range correct switch and an inverter. The inverter output is $-R_a$ which is fed to the range correction circuit, the range correct switch and another inverter. This inverter output is $+R_a$ which is fed to the range correction circuit.

The output of the last inverter is identical to the output of the integrator when it is integrating, but during the idle time between integrations the output of the inverter is held at a positive DC level while the output of the integrator is allowed the slight drift which is normal to an op amp. This prevents the inverter from ever feeding a negative voltage to the multiplier on the range correction module where it would cause a phase reversal making the range correction circuit unstable.

The signal +R is fed to the end-sweep-logic module from the range correct switch (R can be either $+R_a$ or $+R_c$ depending

on the position of the range correct switch). The end-sweep-logic module detects when the ramp voltage +R reaches +10 volts in amplitude and changes the logic level to turn off the integrator.

The slope of the ramp generated by the integrator determines the time it takes the ramp to reach a magnitude of +10 volts, which determines the range scale on the PPI. The slope depends on the value of input resistance to the integrator. This value is determined by a four-position switch on the front panel which selects the input resistor for the range scale desired.

B. RANGE CORRECTION CIRCUIT

The range correction circuit, Fig. 6, receives $+R_a$ signals from the integrator and the inverter mentioned above. It also receives the signal +y which is fed back from the output circuit. The range correction module output is $+R_c$ which is inverted to $-R_c$. Both $+R_c$ and $-R_c$ are fed to the range correct switch in the output circuit.

C. FEATHER CIRCUIT

The feather-circuit block diagram is shown in Fig. 7. The pulses received at the feather input are increased in duration by the pulse stretcher. The stretched pulses are fed to the sample and hold where they are sampled each time a one microsecond pulse is received from the one-shot module. The hold portion of the circuit feeds its output to the height-to-width converter, which also receives an input from

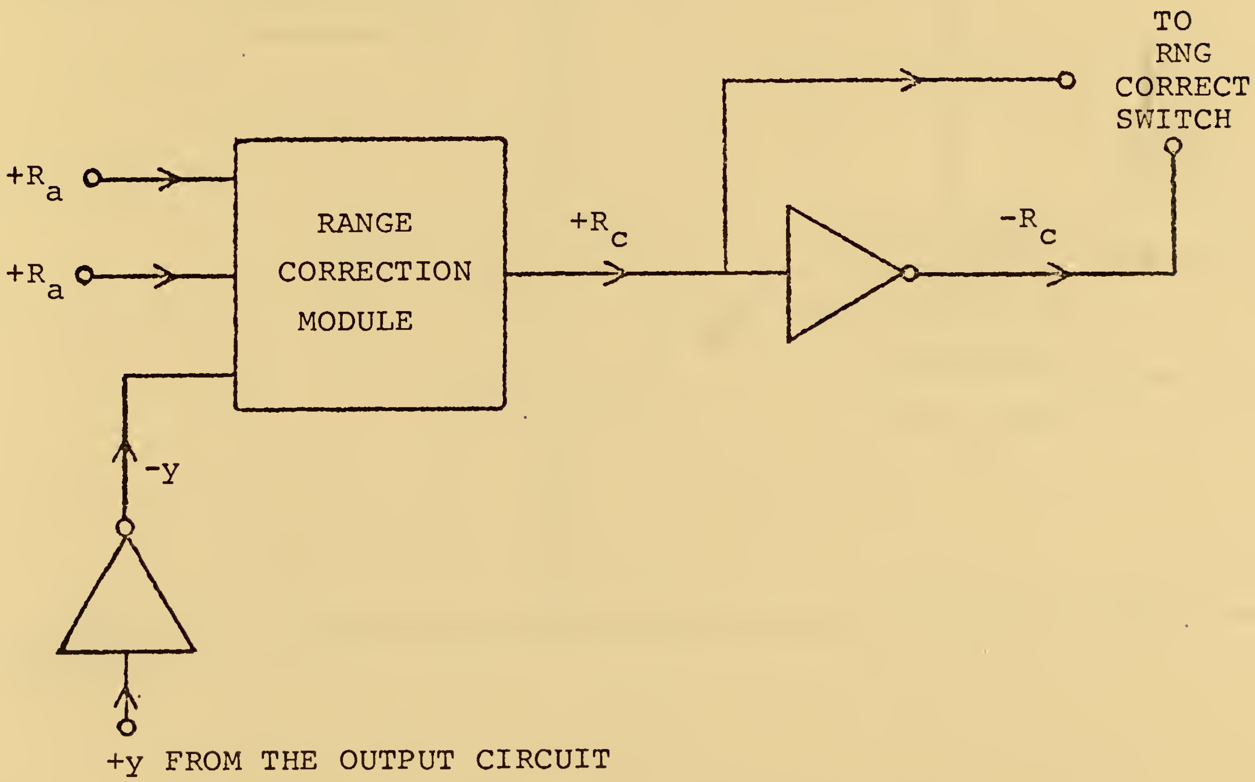


Figure 6. Range Correction Circuit.

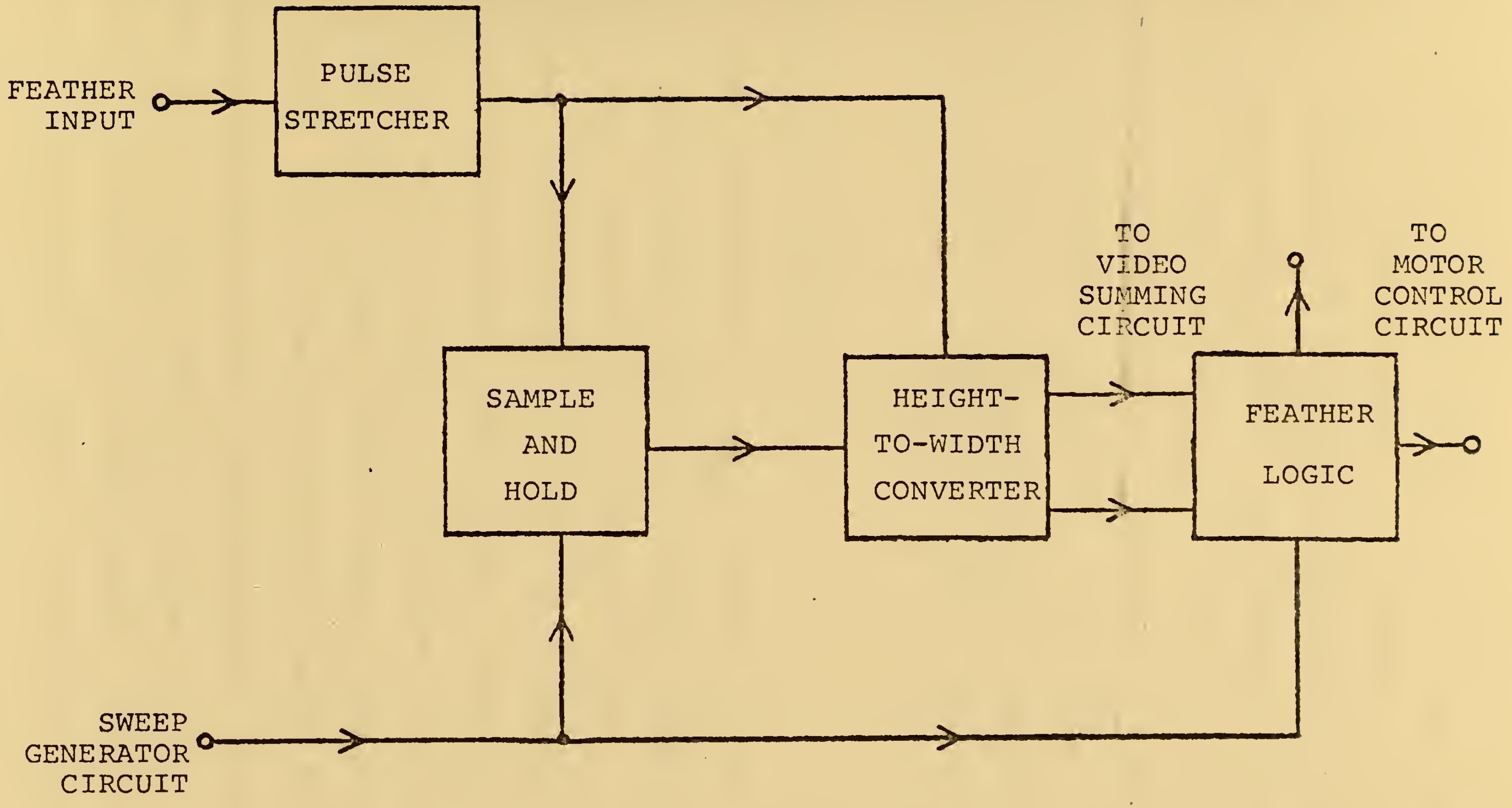


Figure 7. Feather Circuit.

the pulse stretcher and $+R_a$ from the integrator. The height-to-width converter output consists of two logic signals which it feeds to the feather circuit. The duration of the logical one pulses in these two signals is dependent on the magnitude of the stretched feather pulse. The feather circuit uses the two logic signals in conjunction with the one microsecond pulse from the one shot to determine if the receiver is being illuminated by the main lobe of a radar. The feather logic outputs are a logic level to the motor control circuit and a logical one pulse of video to the output circuit.

D. MOTOR CONTROL CIRCUIT

The motor speed-control circuit block diagram, Fig. 8, shows that the azimuth-ramp and DC-voltage generator module receives a logic input from the feather circuit. It generates a linear ramp voltage the magnitude of which is proportional to the transmitting radar antenna rotational period, and a DC level which is equal in magnitude to the maximum value of the ramp voltage. The DC level is applied to the linear portion of the sine/cosine potentiometer which is being rotated by the DC motor. The output of the sine/cosine potentiometer is a ramp voltage the slope of which is proportional to the motor's rotatonal period. The azimuth ramp has a constant slope, and the sine/cosine ramp has a constant maximum magnitude which is equal to the maximum magnitude of the azimuth ramp. Therefore if the speed of

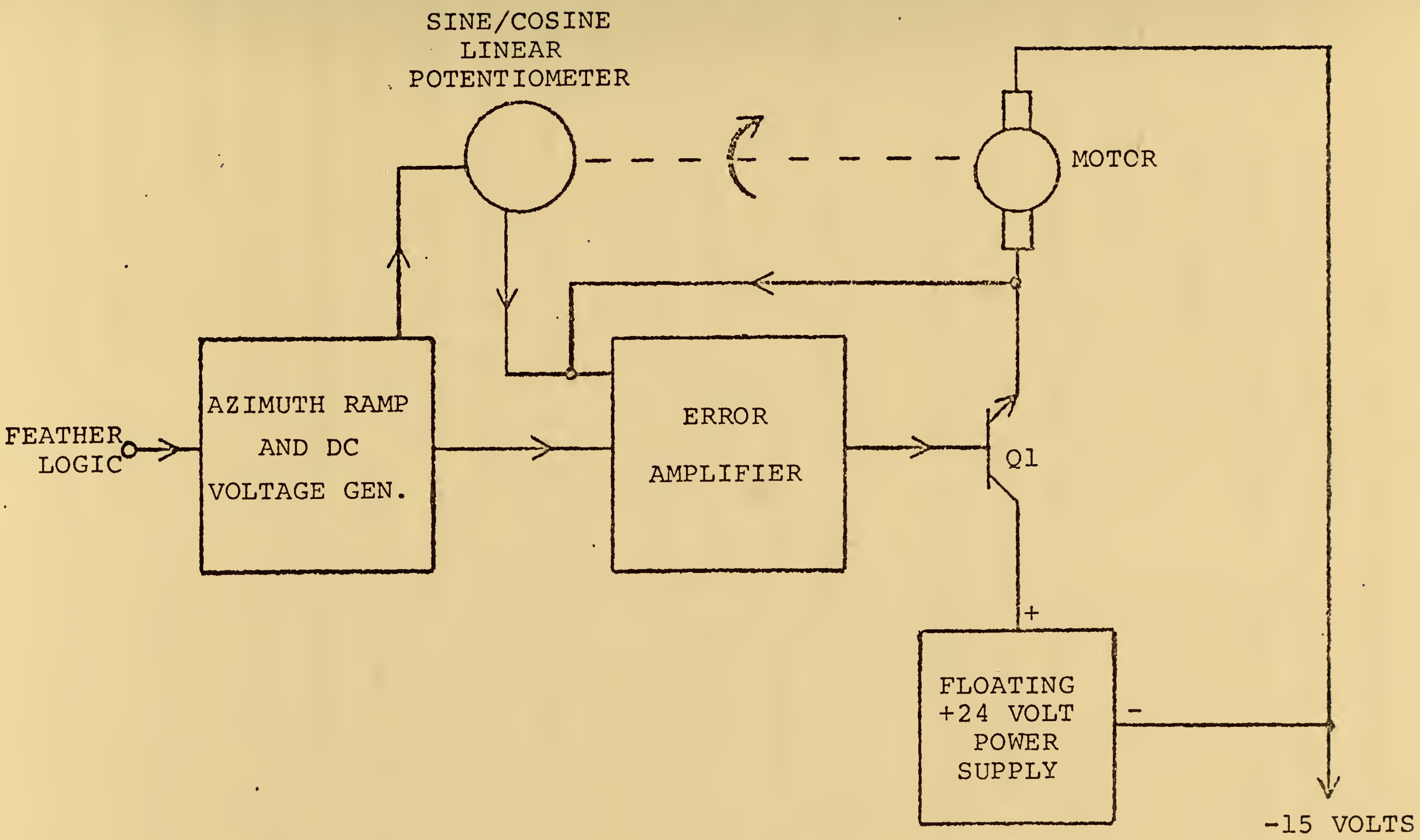


Figure 8. Motor Speed Control Circuit.

the motor is changed until the two ramps are identical, the motor and the transmitting antenna must have identical rotational periods. The ramps are subtracted in the error amplifier, and the difference is amplified and fed to the DC motor to correct the motor speed so that it is identical with that of the antenna.

E. OUTPUT CIRCUIT

The block diagram for the output circuit is shown in Fig. 9. It has two distinct and separate portions, but they both furnish outputs which are applied to the PPI display.

The video summing amplifier combines the intensity, feather, video and range marks inputs and furnishes them as both +Z and -Z outputs in order to have the correct signal polarity available for the Z axis of any X-Y display used as a PPI.

The other circuit contains the range-correct switch which is a DPDT switch that permits selection of either corrected or uncorrected range voltages, $\pm R_c$ or $\pm R_a$, for application to the sine/cosine potentiometer. The outputs of the sine/cosine potentiometer, $y = R \cos \phi$ and $x = R \sin \phi$, are buffered and then transmitted to the X and Y inputs of the PPI display.

F. BUILT-IN-TEST SIGNAL GENERATOR

Figure 10 is the block diagram of the built-in-test signal generator circuit. This circuit generates a 500 Hz

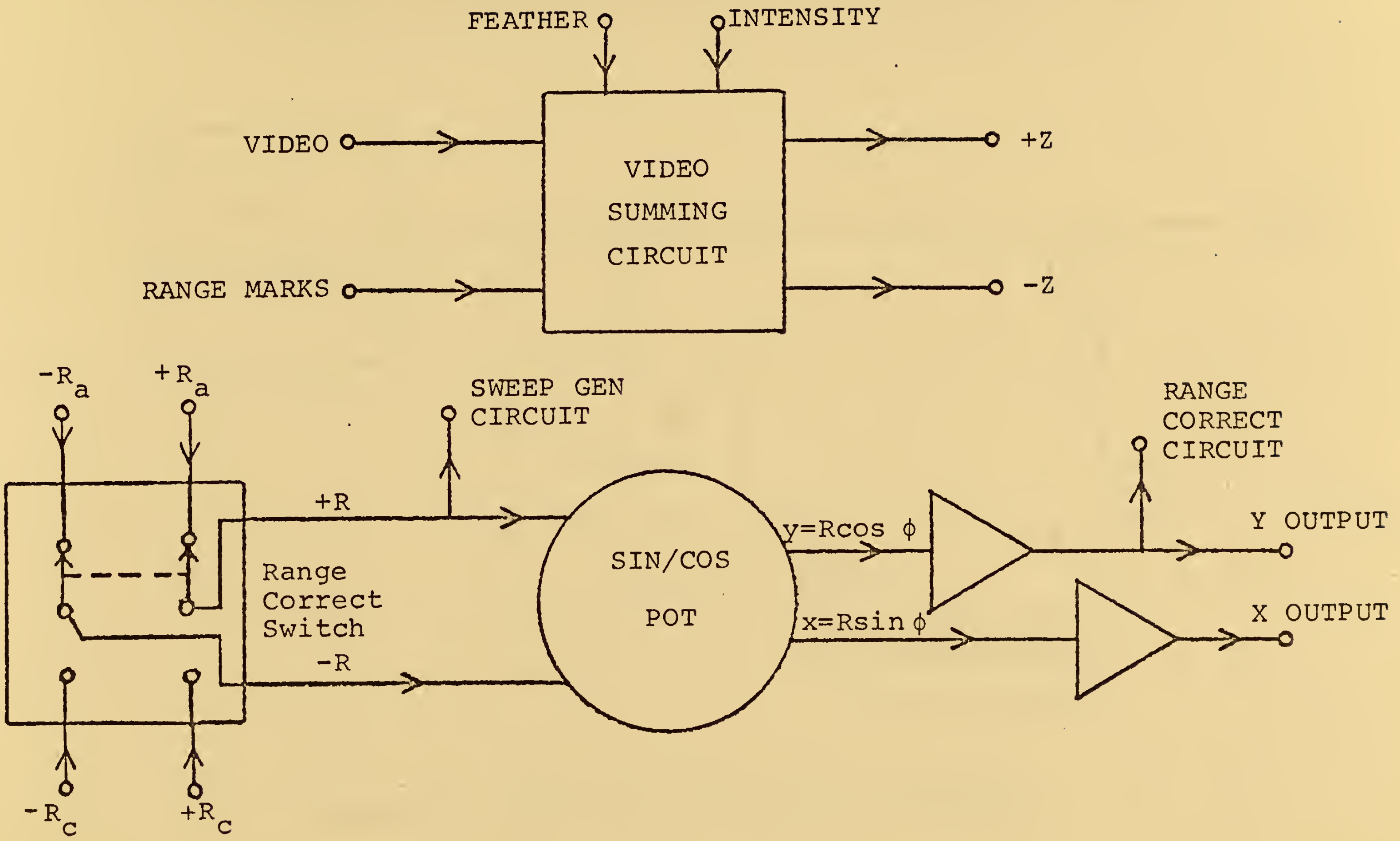


Figure 9. Output Circuit.

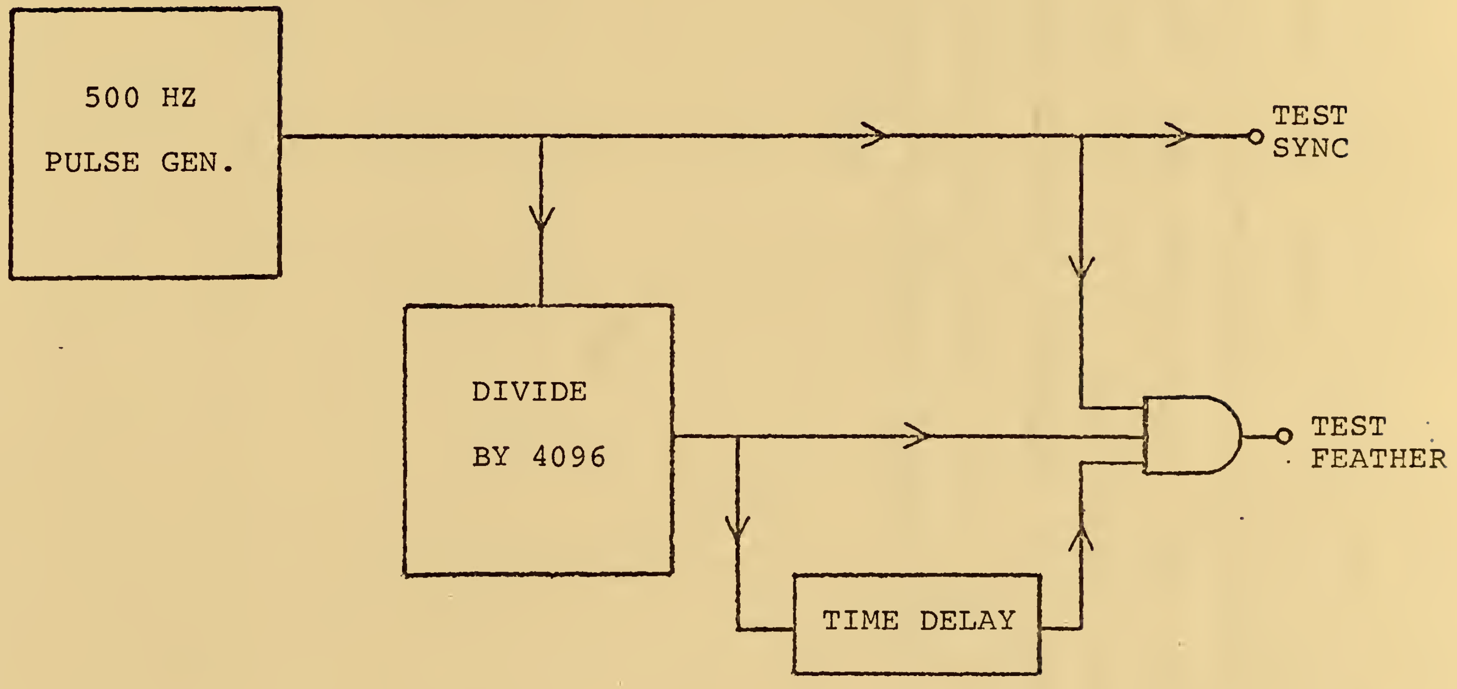


Figure 10. Built-in-test Signal Generator.

pulse train as a test sync signal. The pulse train is passed through a divide-by-4096 circuit and from there through a time-delay circuit. The outputs of the pulse generator, the divide circuit and the time delay are then combined in an "AND tie" to give a test feather signal. The "AND tie" is simply the physical wiring of the three outputs together. This has the effect of using an AND gate. The outputs of the circuit simulate a radar signal, with a PRF of 500, which is illuminating the bistatic receiver with its main lobe every eight seconds.

IV. OPERATING CONTROLS, INPUTS AND OUTPUTS

All the controls necessary for operating the bistatic radar processor are located on the front panel. The rear panel contains all the input and output connectors and the switch to activate the test signal generator.

A. FRONT PANEL

The controls shown on the front panel view in Fig. 11 should be operated in the following manner to obtain optimum performance from the processor. All adjustments assume a radar signal is being received and fed to the processor inputs.

1. Threshold Set

The threshold set adjustment is made in order to insure that the processor is being triggered only by the received radar's PRF signal and not by target returns and noise.

Rotate the threshold set knob clockwise until the PPI display goes blank. This increases the threshold voltage magnitude to a value greater than the magnitude of the incoming radar signal. Now, slowly rotate the knob counterclockwise just until the PPI display lights up again. The processor is now being triggered only by the strongest signal being received, which should be the radar's PRF signal.

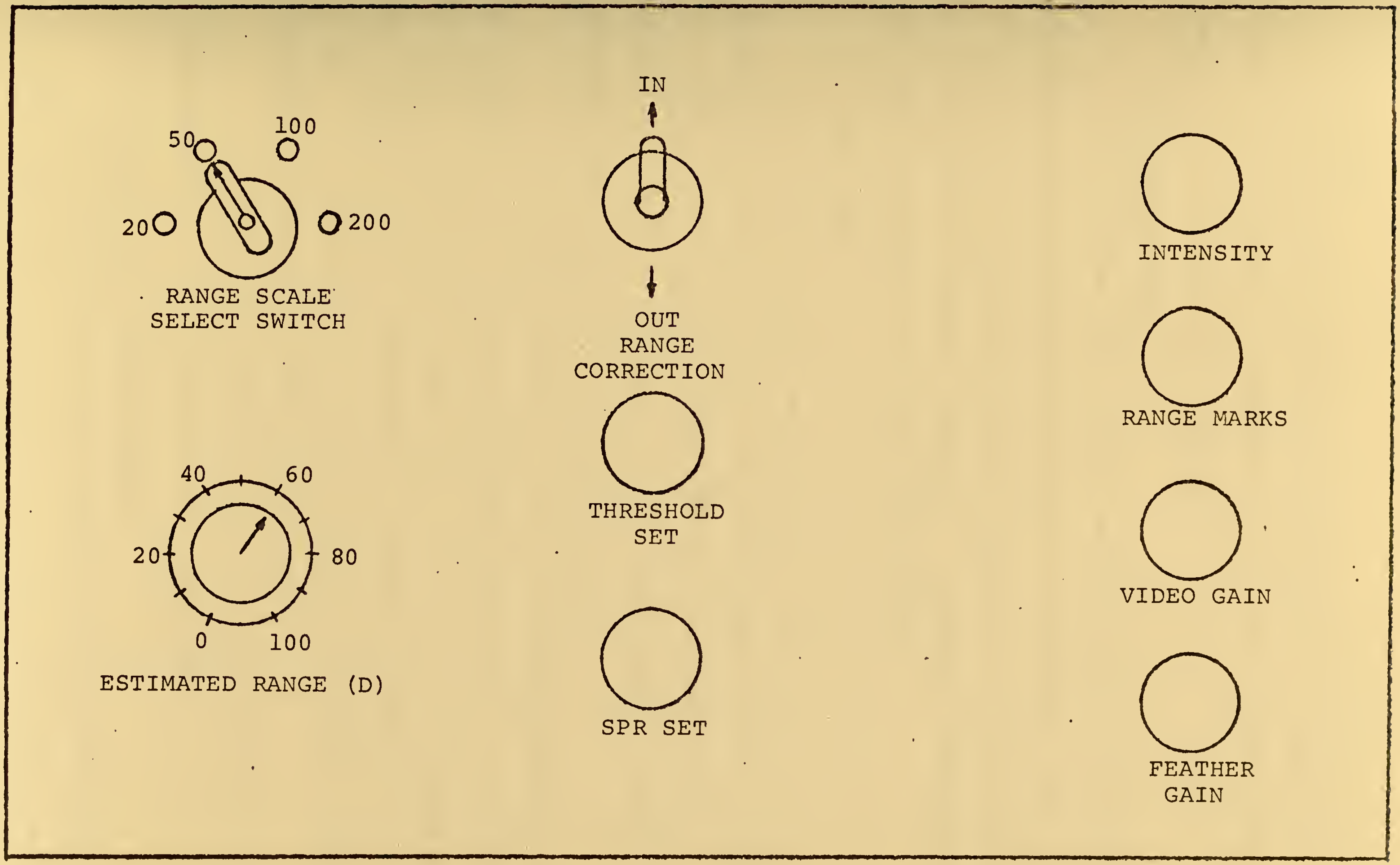


Figure 11. Processor Front Panel.

2. Gain

Adjust the intensity, range marks and video gain knobs for optimum PPI display presentation. Turning the knobs clockwise increases the gain.

3. Feather Gain

The feather gain control adjusts the width of the feather on the display rather than the intensity. The feather can be removed from the display by rotating the knob in the counter-clockwise direction. Clockwise rotation of the knob increases the width of the feather.

4. SPR Set

The SPR (seconds per rotation) set control is a manual adjustment to assist the motor speed control circuit in synchronizing the PPI display with the transmitting antenna rotation. Judicious use of this control can minimize the time required for synchronization.

If the radar picture on the PPI display appears to be rotating in a clockwise direction the motor is going too fast and needs to be slowed down. This can be accomplished by rotating the SPR set knob in a counter-clockwise direction. If the picture is rotating counter-clockwise, rotate the knob clockwise to speed up the motor.

Once the motor speed is near the speed of the antenna the automatic control circuit will take over.

5. Range Scale Select Switch

The range scale select switch is self explanatory. If range correction is going to be used, this switch must be in the 50 mile range scale position since that is the only

range scale which has range correction. A display picture is still present when different range scales are selected for range correction, but the range correction circuit output is erroneous.

6. Range Correction

Range-correction mode of operation is selected by placing the DPDT switch in the up or in position.

The estimated range knob should be set at the best estimate of the range between the transmitting antenna and the bistatic radar receiver. This setting is not very critical but should be made as accurately as possible.

B. REAR PANEL

Figure 12 shows the rear panel view of the processor. The connectors shown serve the following functions. The sync, video and feather connectors are for inputs to the processor from the bistatic radar receiver. The 36 pin input/output connector provides connections for the supply voltages and for leads to and from the DC motor and the sine/cosine potentiometer. The X,Y,Z and -Z connectors are for outputs from the processor to the X-Y display unit.

The DPDT switch on the rear panel selects either radar inputs to the processor or inputs from the built-in test signal generator circuit.

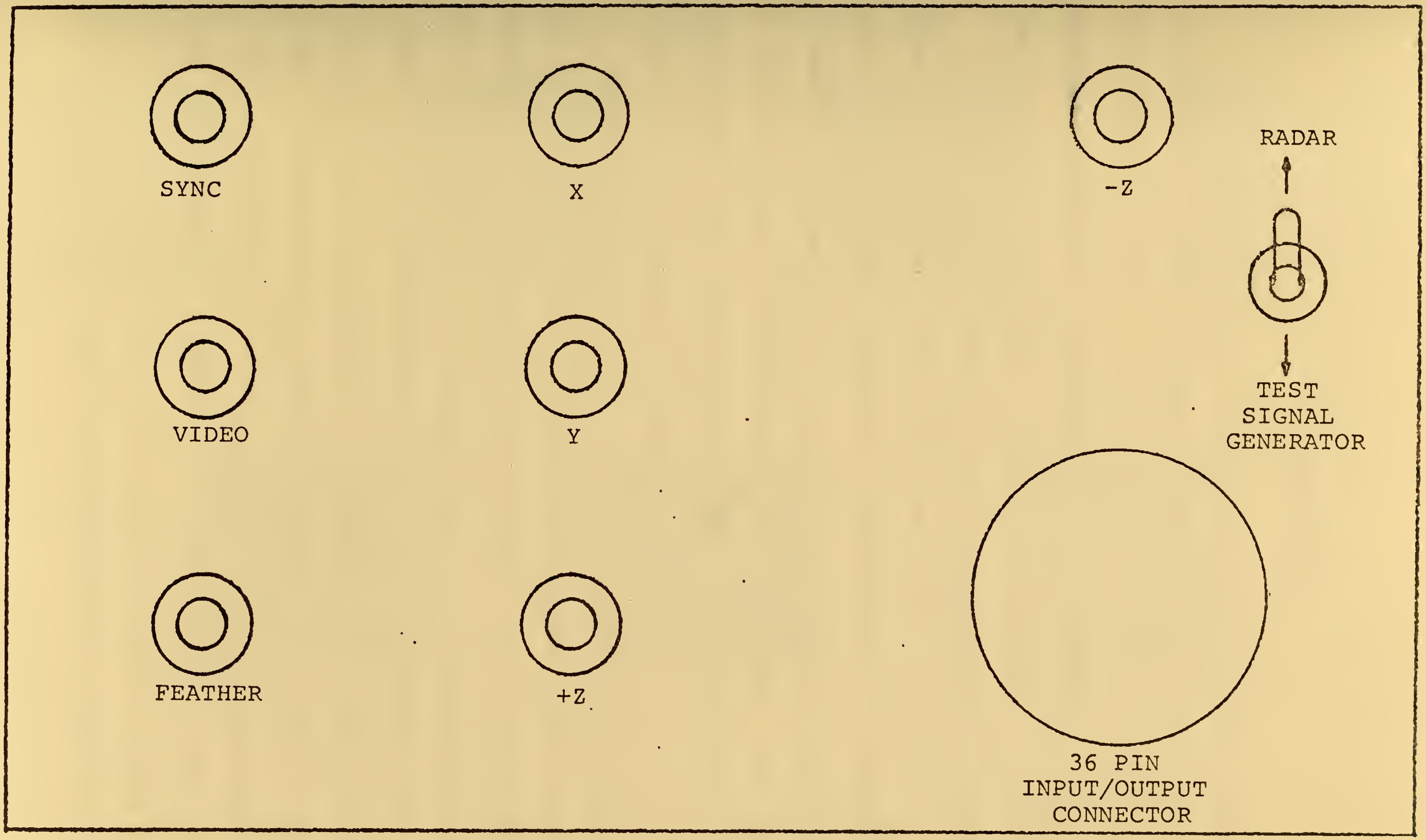


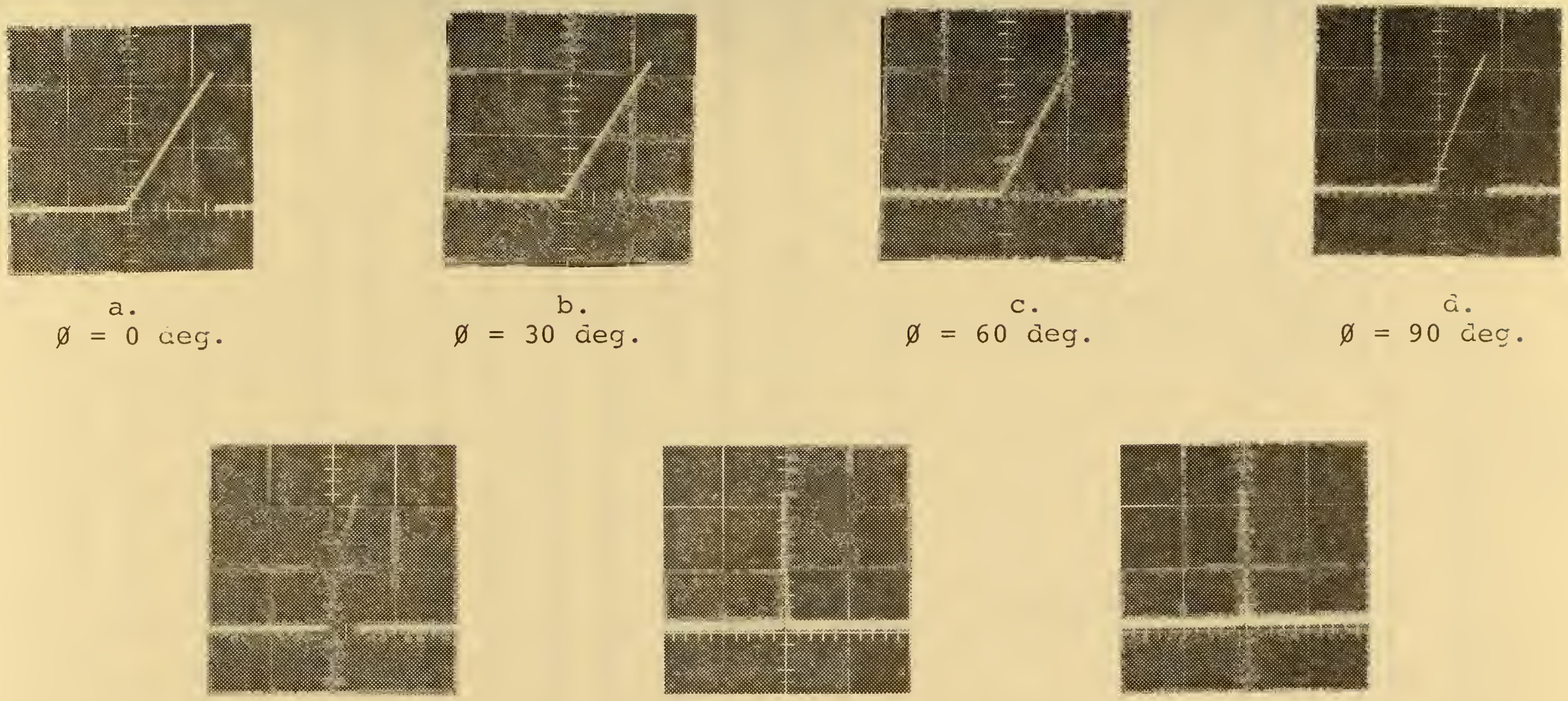
Figure 12. Processor Rear Panel.

V. CONCLUSIONS

The range correction method utilized in this processor is superior to the one used in the processor built by NAFI. The present circuit is more capable of making the instantaneous increases in voltage which are necessary for range correction in the region from $\phi = 135$ degrees to 225 degrees.

Figures 13a through 13g are oscilloscope photographs showing the output of the range correction circuit, R_c, for angles of ϕ of zero degrees to 180 degrees in 30 degree increments. Processing methods and waveforms in the region from 360 degrees to 180 degrees are identical. The photographs were taken with the processor in the 50 mile range scale and for D equal 100 miles.

Figure 13a is used as a reference since the waveform of R_c is identical to the uncorrected apparent range voltage waveform, R_a, at ϕ equal zero degrees. As ϕ is increased, Fig. 13b through 13g, the waveform of R_c becomes more non-linear and the required time to reach a magnitude of +10 VDC, the voltage which corresponds to a range of 50 miles, is reduced; see Table I column two. This is caused by the requirement for increasingly larger range corrections as ϕ approaches 180 degrees. The waveforms in Fig. 13f and 13g do not display their non-linearity because range correction in that region requires instantaneous increases in



a.
Ø = 0 deg.

b.
Ø = 30 deg.

c.
Ø = 60 deg.

d.
Ø = 90 deg.

e.
Ø = 120 deg.

f.
Ø = 150 deg.

g.
Ø = 180 deg.

Figure 13. Oscilloscope photographs of the range correction circuit output. The oscilloscope scales are set at five volts/cm and 0.5 msec/cm.

TABLE I

COMPARISON OF THEORETICAL AND MEASURED RANGES FOR THE RANGE CORRECTION CIRCUIT

Angle (degrees)	Time to Reach 10 Volts (micro sec)	Measured Range R_a (miles)	Theoretical Range R_a (miles)
0	625	50	50
30	600	48	47.3
60	525	42	39.6
90	350	28	28
120	200	16	15.5
150	-	-	4.3
180	-	-	0.0

voltage so large that a magnitude of +10 VDC, and cutoff, is reached before the non-linearity becomes apparent.

Table I is a comparison of the theoretical and measured values of uncorrected apparent range voltage, R_a, which will give R_c = 50 miles at the values of ϕ listed. This table shows that as ϕ approaches 180 degrees the apparent range required to yield a corrected range of 50 miles grows smaller and smaller. Theoretically at ϕ equal 180 degrees the value R_a equal zero yields R_c equal 50 miles. However, due to the finite response time of the range correction circuit, this occurs at some angle between 150 and 180 degrees. The result is that no targets will appear on the PPI display in the region from this angle to 180 degrees. The angle at which this occurs can be pushed closer to 180 degrees as electronic

components with faster response times become available for the range correction circuit.

Another phenomenon which occurs is a marked reduction in range resolution in the region near 180 degrees. This is caused by the relatively smaller differences in direct path between transmitter and receiver and reflected path from transmitter to target to receiver which occurs for targets in this region. It is evidenced by a radial elongation of target returns and even more dramatically by the increased thickness of the range rings in this region. There is no solution to this problem as it is inherent to the separation of the transmitting and receiving antennas.

Of the two methods for generating the PPI sweep mentioned in section II.C, the one used in NAFI's processor is the more desirable. This method utilizes a crystal oscillator and generates the sweep digitally, as opposed to the DC motor utilized by the author. The advantage to NAFI's method is that, since it is completely electronic, it does not have the slow response times and non-linearities inherent to the DC motor. It synchronizes almost instantaneously and it does not have a hunting problem. However, NAFI's method is much more expensive and produces a larger and heavier processor.

A combination of the author's range correction system and NAFI's PPI sweep generation system would appear to be the optimum system.

The motor control circuit would benefit from some redesign work to eliminate the hunting problem and to speed up the synchronization process.

The remaining circuits accomplish their functions as designed, and a successful bistatic radar processor has been built for performance under conditions when size and weight considerations preclude use of a larger more sophisticated system such as NAFI's. The author's processor would be ideal for use as a portable system since it could be contained, with a small X-Y display, in an attache-case sized package.

APPENDIX A

INPUT POWER CONNECTOR (MODULE A1)

The input-power connector module was developed by NAFI to deliver the power required by all modules in a single card cage assembly from a suitable power supply. Discussion of this module was taken from Ref. 1.

Because the power connector was designed for use in units relying heavily on transistor-transistor logic (TTL), a large current at five volts was required. For this reason six pins were bussed together inside the connector and AWG No. 18 wire was used permitting a current as high as six amperes.

The other voltages required by the modules (±15 volts) were allotted two pins each using AWG No. 26 wire on each pin. This provides for a maximum of two amperes. In order to provide a good ground for these voltages, another buss connecting eight pins is provided using AWG No. 16 wire. AWG No. 26 wires were used on the remaining pins because of the low power requirements.

Table II shows the pin numbers of each wire, its color code, its function and where it is connected.

TABLE II

INPUT POWER CONNECTOR

Pin #	Color	Function	Connection (pin #)
1	Red	+15 VDC	Rear pwr connector (K)
2	Wh/Blk/Yel		Test signal switch (5)
3	Blk	GND	Rear pwr connector (J)
4			
5			
6			
7			
8			
9			
10			
11	Blk	Chassis GND	Chassis
12	Wh/Blk/Blu		Threshold set pot (2)
13	Red	+5 VDC	Rear pwr connector (L)
14			
15			
16			
17			
18			
19	Wh/Blk/Grn		Sync input (GND)
20	Violet	-15 VDC	Rear pwr connector (H)
21	Red	+15 VDC	Rear pwr connector (K)
22	Brown		Range select switch (1)
23	Orange		Range select switch (2)
24	Yellow		Range select switch (3)
25	Green		Range select switch (4)
26	Blue	$+R_a$	Range correct switch
27	Gray	$-R_a$	Range correct switch
28	White	$+R_c$	Range correct switch

TABLE II (Continued)

Pin #	Color	Function	Connection (pin #)
29	Wh/Blk	$-R_c$	Range correct switch
30	Wh/Red	Spare	Rear pwr connector (G)
31	Wh/Or	R sin ϕ	Rear pwr connector (Z)
32	Wh/Yel	R cos ϕ	Rear pwr connector (a)
33	Wh/Grn		X (Center)
34	Wh/Blu		Y (Center)
35	Wh/Vio		X (GND)
36	Wh/Gray		Y (GND)
37	Wh/Blk/Brn		Video gain pot (2)
38	Wh/Blk/Red		Video gain pot (1)
39	Wh/Blk/Or		Range select switch (GND)
40	Violet	-15 VDC	Rear pwr connector (H)

APPENDIX B

INPUT CONNECTOR (MODULE A2)

The input connector was developed by NAFI to provide a direct link between the circuitry built into standard hardware and the inputs, output and controls that are used in conjunction with the circuitry. Discussion of this module was taken from Ref. 1.

Due to the large number of wires, the comparatively small size of the connector, and the generally low power requirements of standard hardware, AWG No. 26 wires were chosen as the most practical size. To aid in assembly and trouble-shooting, each wire is stamped with the number of the pin on the connector to which it is soldered.

Table III shows the pin number of each wire and where it is connected.

TABLE III

INPUT CONNECTOR

Pin #	Connection (pin #)
1	NC
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
10	NC
11	NC
12	NC
13	SPR pot (1)
14	SPR pot (3)
15	SPR pot (2)
16	Motor control transistor Q1 emitter
17	Motor control transistor Q1 base
18	Sin/cos linear pot (wiper)
19	Sin/cos linear pot (CCW)
20	Sin/cos linear pot (CW)
21	Range correct switch (+R)

TABLE III (Continued)

Pin #	Connection (pin #)
22	Estimated range pot (1)
23	Estimated range pot (2)
24	Threshold set pot (3)
25	Threshold set pot (1)
26	Sin/cos pot (GND)
27	Test-signal switch (3)
28	Test-signal switch (4)
29	-Z (GND)
30	-Z (Center)
31	+Z (GND)
32	+Z (Center)
33	Intensity pot (3)
34	Intensity pot (2)
35	Intensity pot (1)
36	Range marks pot (3)
37	Range marks pot (2)
38	Test-signal switch (6)
39	Feather gain (1)
40	Range marks pot (1)

APPENDIX C

BUILT-IN-TEST SIGNAL GENERATOR (MODULE A3)

The built-in-test signal generator was designed by the author to provide the test signals required to check out the bistatic radar processor. Side B of the module is blank and is not used. Side A contains five Texas Instruments integrated circuits. They are an SN54L00 low-power quadruple 2-input positive NAND gate, an SN 5405 hex inverter with open collector output and three SN 5493 4-bit binary counters. These integrated circuits are shown in Fig. 14 as Z1 through Z5 in the order listed above. The remaining components in the circuit are R1 and C1 which are feedback components in the oscillator. R2, R3, R5, R6 and R7 are all pull-up resistors to help the various gates achieve logical one level. C2 and R4 are a low-pass filter designed to delay the logic level changes to pin two of Z1. C3 serves to delay the logic level transitions at pin five of Z2.

The block diagram in Fig. 15 and the waveforms in Fig. 16 will aid comprehension of how the test signal generator performs its function. In Fig. 16a the waveforms apply to the portion of the circuit prior to the divide by 4096 while in Fig. 16b the waveforms, which are plotted to a different time scale, apply to the portion of the circuit following the divide by 4096.

R1, C1 and NAND gates G1 and G2 form a multivibrator which has a 500 Hz output that is represented by the waveform in Fig. 16a(1). Inverter one inverts the signal, Fig. 16a(2),

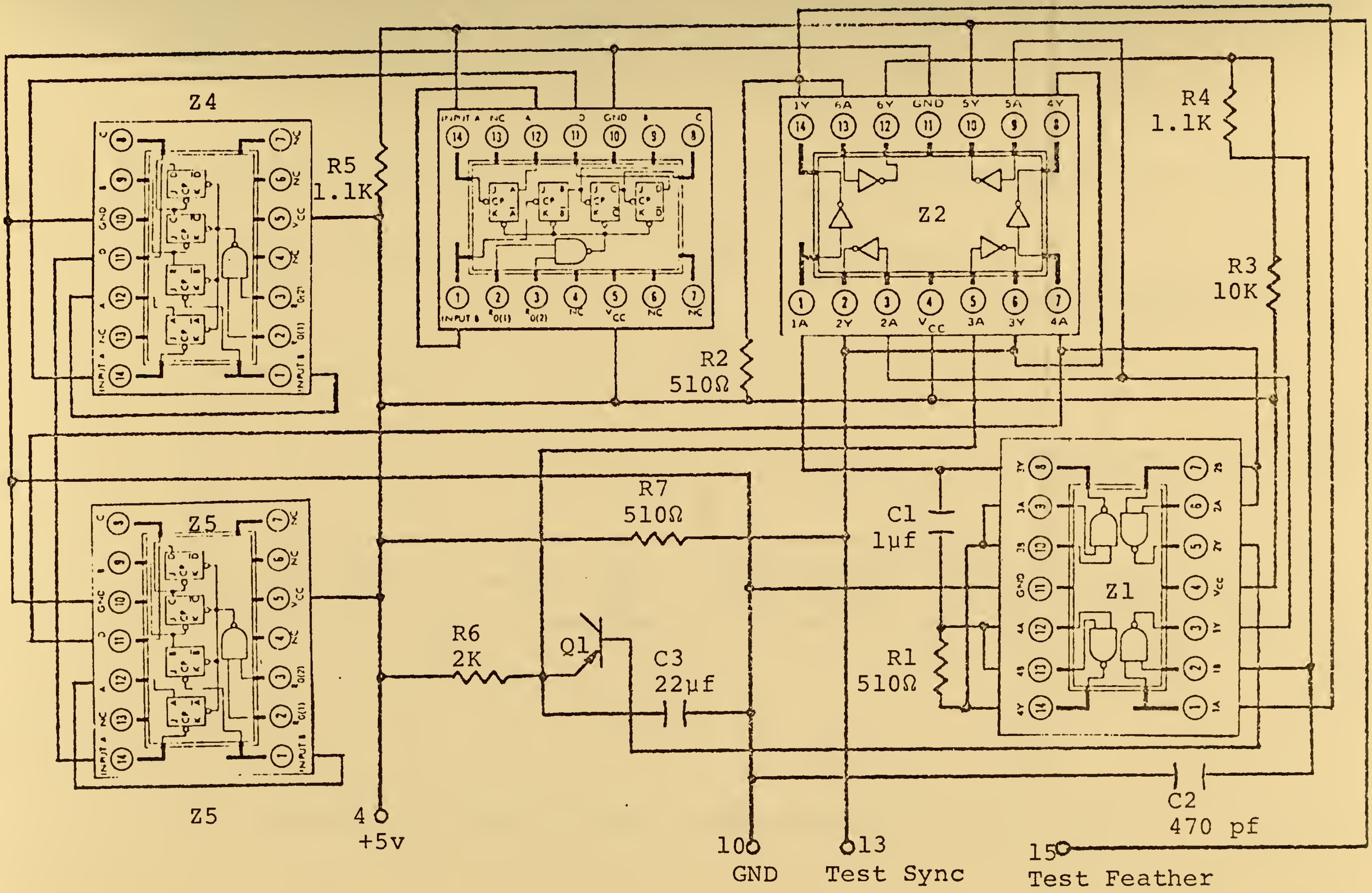


Figure 14. Built-in-test Signal Generator Module - Side A.

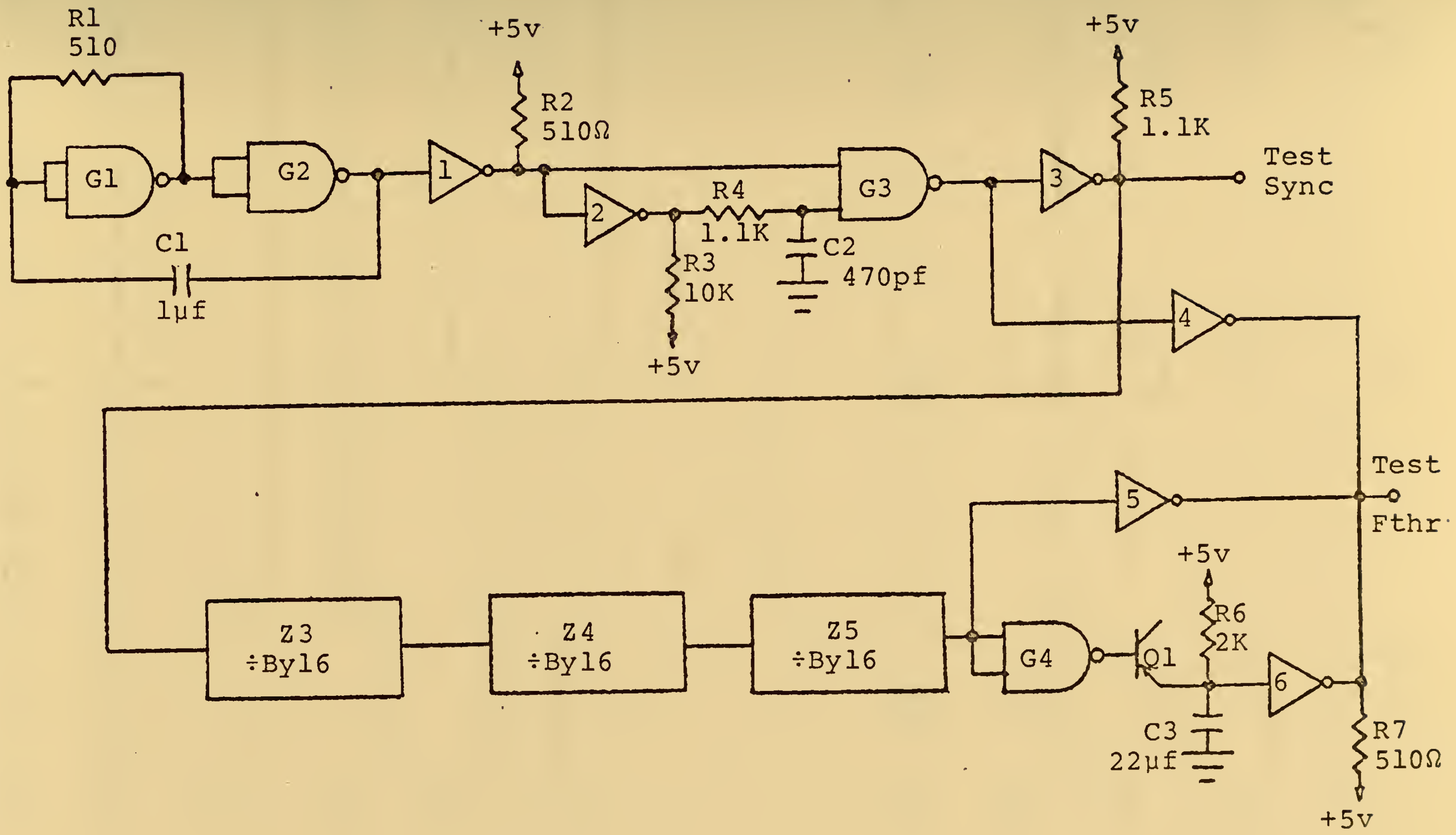


Figure 15. Built-in-test Signal Generator Block Diagram.

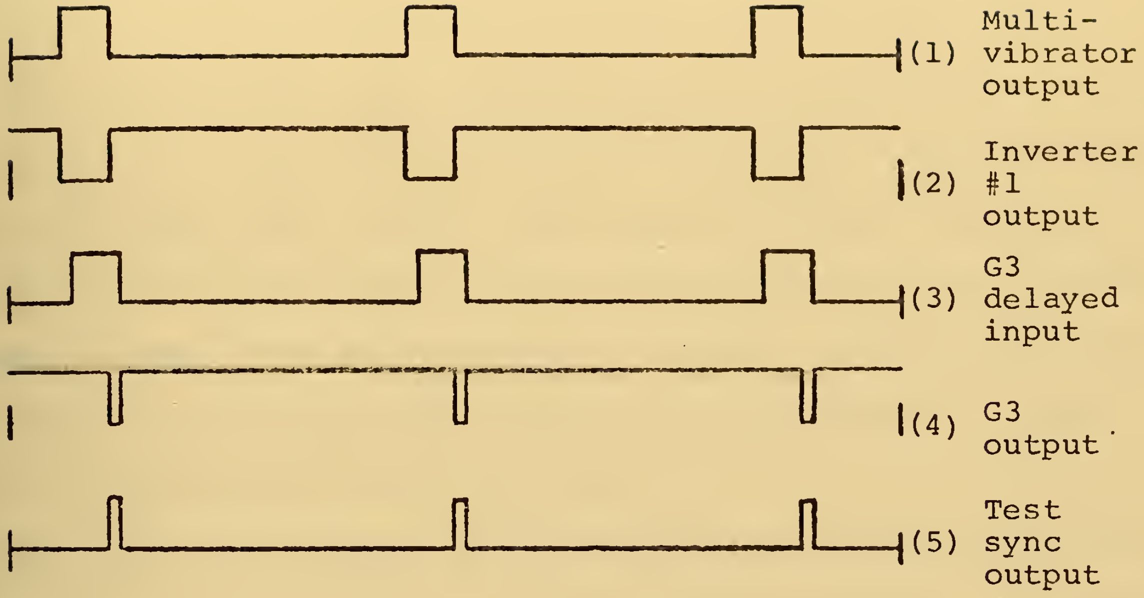


Figure 16a

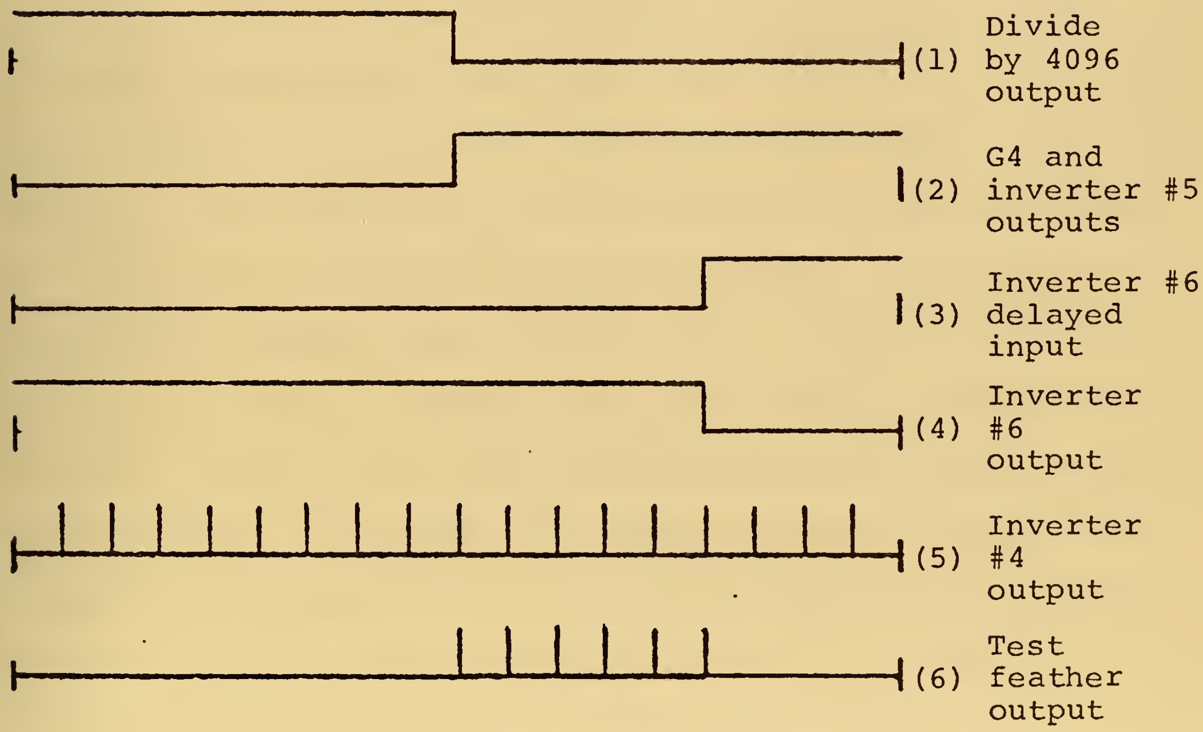


Figure 16b

Figure 16. Test Signal Generator Waveforms.

and feeds it to G3 and inverter two. Inverter two inverts the signal and feeds it through the delay network to G3. This input to G3, Fig. 16a(3), is delayed slightly as can be seen by comparing its waveform with the waveform of the other input, Fig. 16a(2). The output of G3 is a logical zero pulse, Fig. 16a(4), which occurs only when both inputs are logical one simultaneously. Inverter three inverts this signal, Fig. 16a(5), and feeds it to the test sync output as a 500 Hz positive pulse train.

The 500 Hz signal is also fed through the divide-by-4096 circuit which provides a 0.122 Hz output signal. Since this low-frequency signal waveform cannot be easily shown, only the portion of the waveforms that are critical to the operation of the circuit are shown in Fig. 16b.

Figure 16b(1) shows the output of the divide-by-4096 circuit as it makes a transition from logical one to logical zero. Both G4 and inverter five invert the signal, Fig. 16b(2). The output of G4 is fed through the delay network to the input of inverter six, Fig. 16b(3). Inverter six inverts the signal, Fig. 16b(4). The outputs of inverter four, Fig. 16b(5), inverter five, Fig. 16b(2), and inverter six, Fig. 16b(4), are "AND tied" to the test feather output of the module. The "AND tie" output, which is logical one only when all three of its inputs are logical one, is shown in Fig. 16b(6). The test feather output is a burst of several pulses every eight seconds.

APPENDIX D

TEST POINTS (MODULE A4)

The test-point module is a general purpose unit which, when utilized properly, will allow a circuit malfunction to be isolated to a few or even one discrete module. The discussion of this module was taken from Ref. 1.

The module contains 40 test points. Each of the selected test points throughout the system is fed to a pin on the wirewrap plate below the module, then each signal is brought from the wirewrap plate through printed circuit paths on the module to a female connector mounted on top. This permits convenient monitoring of the signals with an oscilloscope and pointed probe adapter.

Table IV shows the test-point module pin numbers, the module and pin number of the test point and the signal being tested.

TABLE IV

TEST POINT MODULE

Pin #	Test Points Module-Pin#	Signal Tested
1	B1-21	Sync input
2	B1-27	Threshold detector output
3	B2-3	One shot output (360 microsecond)
4	B3-15	Logic level to start (stop) integrator
5	B3-4	+R input to end sweep logic
6	B4-9	$+R_a$ output from integrator
7	B5-18	$-R_a$ output from inverter
8	B5-5	$+R_a$ output from inverter
9		NC
10	B8-18	-y input to range correction circuit
11		NC
12	B8-19	-z from range correction circuit
13	B8-6	Output of range correction multiplier
14	B8-8	$+R_c$ output from range correction ckt
15	B6-18	$-R_c$ output from inverter
16	B5-26	R sin ϕ from sin/cos pot
17	B5-23	X output
18	B5-37	R cos ϕ from sin/cos pot
19	B5-36	Y output
20	B7-23	Intensity input to summer
21	B7-24	Video input to summer

TABLE IV (Continued)

Pin #	Test Points Module-Pin#	Signal Tested
22	B7-25	Range marks input to summer
23	B7-26	Feather input to summer
24	B7-27	Blanking input to summer
25	B7-33	+Z output
26	B7-36	-Z output
27	B10-34	Feather input from rear panel
28	B10-37	Stretched feather pulse
29	B2-19	One shot output (one microsecond)
30	B11-18	Sampled feather pulse
31	B11-22	Height-to-width logic output
32	B11-26	Height-to-width video output
33	B10-20	Logic output of feather logic circuit
34		NC
35		NC
36		NC
37		NC
38		NC
39		NC
40		NC

APPENDIX E

THRESHOLD DETECTOR (MODULE B1)

The threshold detector used in this bistatic radar processor was developed by NAFI as the line-receiver module which is described in Ref. 1. It accepts a video signal from a bistatic radar receiver, compares the magnitude of the pulses received with a threshold voltage which is manually set with a knob on the front panel of the processor, and provides standard logic outputs with active pull-up from low voltage input pulses. Side A of the module is not utilized. Side B is described in the following paragraphs only so far as it was used in the present application. Those components which were not utilized are not discussed.

The threshold detector functions as an interface between transmission lines and logic circuitry. It utilizes one half of a Fairchild 9615 dual differential line-receiver integrated circuit as shown in Fig. 17. Resistors R1 and R2 provide termination for the input lines. Capacitor C1 provides decoupling for the +5 volt supply and C2 is tied to the response control pin of the 9615 to eliminate outputs for input pulses less than 0.5 microseconds in duration.

One of the two inputs comes from the sync input connector on the rear panel. This input should be a video signal from a receiver tuned to the radar. The other input comes from the threshold set potentiometer on the front panel. The

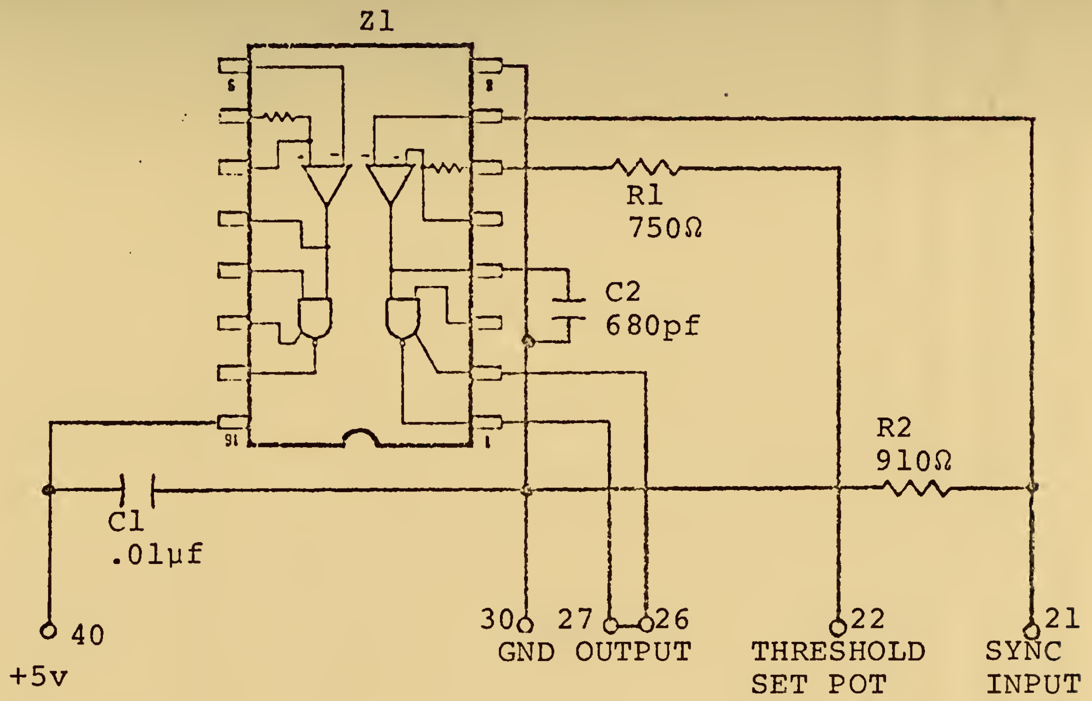


Figure 17. Threshold Detector Module - Side B.

potentiometer provides a DC voltage level which is variable from zero to five volts. This voltage level sets the threshold which incoming radar pulses must exceed before the threshold detector will provide an output. The output goes to one of the one shots on side A of module B2.

It can be seen from the above discussion that noise spikes or other stray signals of less than the threshold voltage in magnitude and/or of less than 0.5 microseconds in duration will not be passed by the threshold detector.

APPENDIX F

ONE SHOT AND RANGE SWITCHING (MODULE B2)

This module was designed by the author. Side A, which consists of two one-shot circuits, provides a 360-microsecond logical one pulse to the height-to-width converter module as the logic input which causes the sample-and-hold circuit to sample its input for one microsecond, and a one-microsecond logical one pulse to the feather-logic module as a clock pulse. These outputs are furnished every time the threshold detector detects the presence of a radar pulse, but no oftener than every 360 microseconds. This limits the maximum radar signal PRF which the processor will handle to about 2700 pulses per second. Side B is a modification of NAFI's range switching logic module which is described in Ref. 1. It allows the selection of one of four different range scales by the range select switch on the processor front panel. When a range is selected with the switch, the range switching logic provides an output which will turn on the correct FET switch on the integrator module so that the DC level input to the integrator is routed through the input resistor for the range scale selected.

On side A, the one-shot circuits each utilize a Texas Instruments SN54121 monostable multivibrator integrated circuit, Z1 and Z2 in Fig. 18. Resistors R1 and R2 and capacitors C1 and C2 are timing components which control

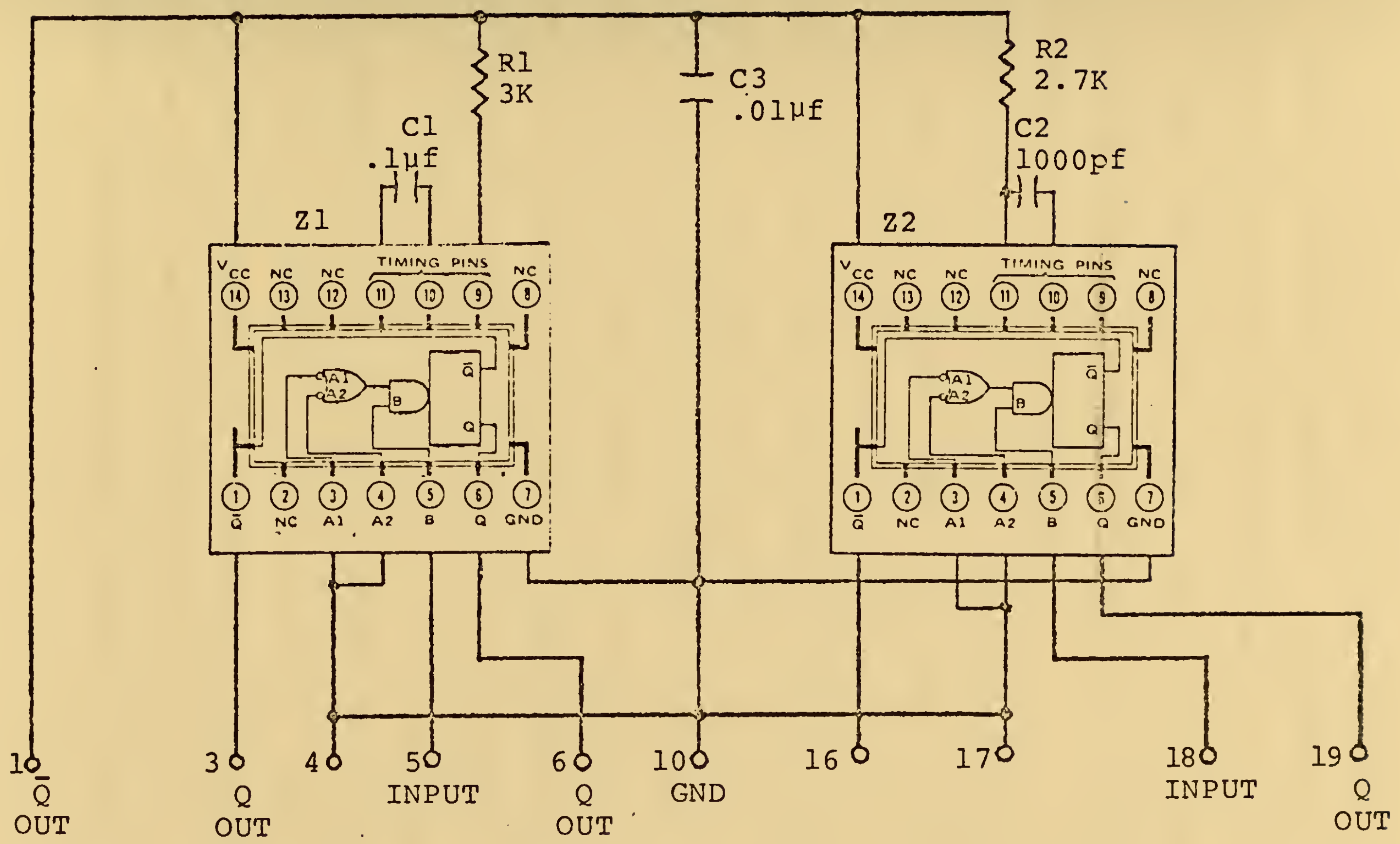


Figure 18. One Shot and Range Switching Module - Side A.

the duration of the output pulses from the two one shots. Capacitor C3 provides decoupling for the +5 volt DC supply.

The first one-shot circuit receives its input, at pin five, from the threshold detector. It provides a Q output at pin six which is the input to the second one-shot circuit, and a $\bar{Q}$ output which goes to pin eight of the end-sweep module. The timing components for this one shot provide a pulse duration of 360 microseconds.

The second one shot receives its input at pin 18 from the first one shot. It provides a Q output at pin 19 which goes to pin 13 of module B10 and pin four of B11. The timing components provide a one microsecond pulse duration.

On side B, the range-switching logic circuit utilizes a Texas Instruments SN5404 hex inverter integrated circuit as shown in Fig. 19. Four of the six inverters are used. R1 through R4 are pull-up resistors to insure that the output of each inverter with a 1.1K resistor, R5 through R8, in series is capable of providing the +1 milliamp maximum drive current required by the FET switch which is to be driven. The 5.1K pull-up resistors, R9 through R12, tied to the inputs of the inverters are to insure a logical one at the inputs when they are not held in the logical zero state. Capacitor C1 provides decoupling for the +5 volt DC supply.

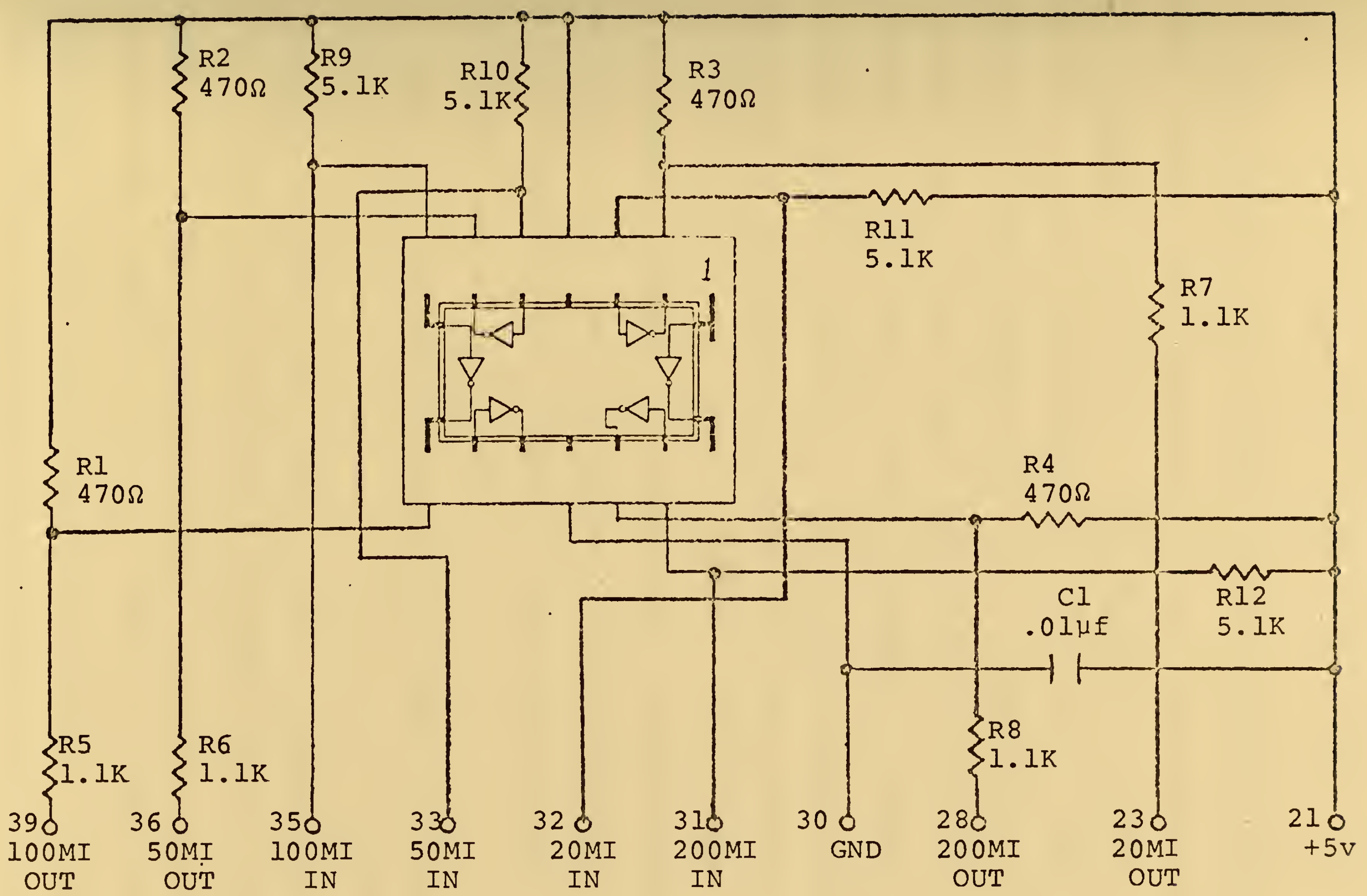


Figure 19. One Shot and Range Switching Module - Side B.

APPENDIX G

END-SWEEP LOGIC (MODULE B3)

The end-sweep logic module was developed by NAFI for their bistatic radar processor and performs the same function in the present application. The discussion of this module was, for the most part extracted from Ref. 1. When sides A and B are interconnected they form a circuit that will, when triggered by a sweep trigger pulse from the one shot module, initiate a logic signal to the integrator to start generating a linear sweep voltage $+R_a$. The circuit detects when the amplitude of R_a reaches +10 volts and then generates a logic level that resets R_a to zero. Another sweep trigger pulse to the module changes the logic level to start another sweep. The circuit also generates pulses of two microsecond duration when the sweep voltage reaches 2,4,6,8 and 10 volts. These pulses are used as range rings.

Side A of the module utilizes two Texas Instruments integrated circuits. They are a SN5495 4-bit right-shift left-shift register and a SN5473 dual J-K master-slave flip-flop. It also uses a Fairchild 710 high-speed differential comparator. These integrated circuits are shown as Z4, Z6 and Z5 respectively in Fig. 20. Side B utilizes a Texas Instruments SN54121 monostable multivibrator, a Siliconix DG123L 5-channel driver with FET switches and a Fairchild 710 shown as Z3, Z1 and Z2 respectively in Fig. 21.

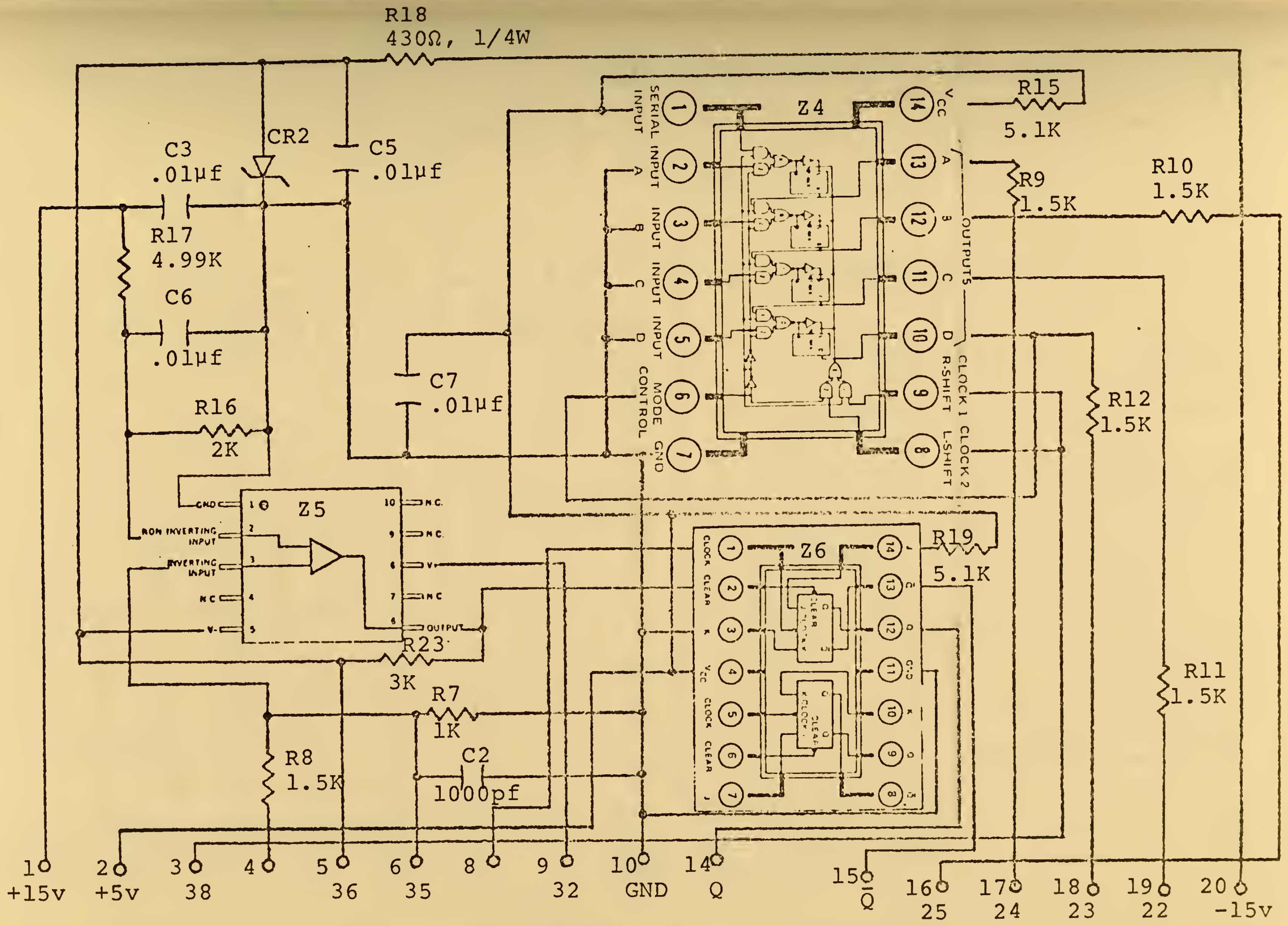


Figure 20. End Sweep Logic - Side A.

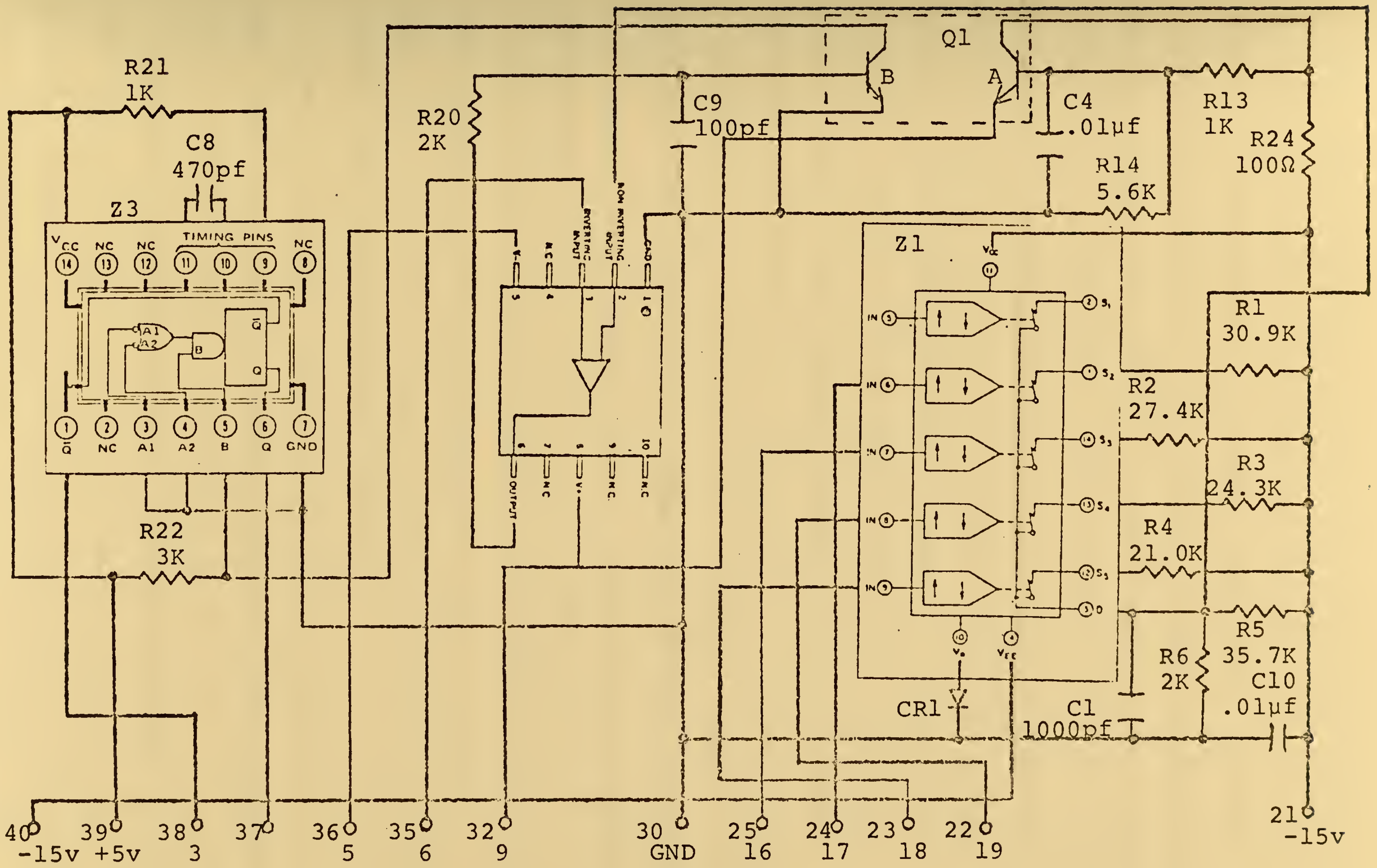


Figure 21. End Sweep Logic - Side B.

The other components on the module have the following functions. Resistors R9 through R12 insure that the maximum input drive current of +1 milliamp required by each FET switch can be obtained. The resistor divider network of R13 and R14 reduces +15 volts DC to approximately +12.7 volts so that the voltage at the emitter of transister Q1-A will be +12 volts. Pins 32 and 9 must be connected together to provide the +12-volt supply potential to both Z2 and Z5. Resistor R18 and zener diode CR2 change -15 volts DC to -6.2 volts. Pins 5 and 36 must be connected together to provide the -6.2 volts supply voltage to both Z2 and Z5. Resistors R20 and R22 and transistor Q1-B through R20 will be inverted at the collector output of Q1-B. Resistor R23 helps pull down the output of comparator Z5 when the output is changing from a logical one to a logical zero. Resistor R24 provides current limiting to the collector of Q1-A. C3, C7 and C10 are decoupling capacitors for the ±15 volt and +5 volt supplies. Diode CR1 from pin 10 of Z1 to ground increases the input switching threshold voltage to the FET switches and increases noise immunity.

There are several low-pass filters to clean up the DC logic levels and supply voltages applied to the integrated circuits in this module. C4 and R9 filter the +12.7 volts on the base of transistor Q1-A. C5 and R18 filter the -15 volt supply voltage. C9 and R20 filter the input signal to the base of Q1-B. C1 and R5 filter the signal to the non-inverting input of comparator Z2. C2 and R8 filter the

inverting input to comparators Z2 and Z5. C6 and R17 filter the non-inverting input of comparator Z5.

The manner in which the module performs its function may be learned by examination of Fig. 22 which depicts the interconnection of sides A and B of the module. The J input to flip-flop Z6 is tied to +5 volts (logical one) through resistor R19, and the K input is tied to ground (logical zero). A sweep trigger pulse, Fig. 23(a), applied to pin eight of the module will cause the Q output (pin 14) of flip-flop Z6 to be a logical one as shown in Fig. 23(b), and the $\bar{Q}$ output (pin 15) to be a logical zero as shown in Fig. 23(c). The $\bar{Q}$ output is used to start a sweep. When the sweep voltage, as shown in Fig. 23(e), is applied to pin four it will be reduced to four tenths of its original value by the resistor divider network of R8 and R7. The reduced sweep voltage, Fig. 23(f), which appears on pin six, is fed to the inverting input of comparator Z5. The resistor divider network of R17 and R16 reduces +15 volts to approximately +4.3 volts. This voltage is fed to the non-inverting input of comparator Z5. When the sweep voltage at the inverting input of comparator Z5 becomes +4.3 volts (approximately 10.7 volts at pin four) the output of comparator Z5 goes from a logical one to a logical zero as shown in Fig. 23(d). The output of comparator Z5 is connected to the clear input of flip-flop Z6. When the clear input of flip-flop Z6 becomes a logical zero, the Q output becomes a logical zero, Fig. 23(b), and the $\bar{Q}$ output becomes a logical one, Fig. 23(c).

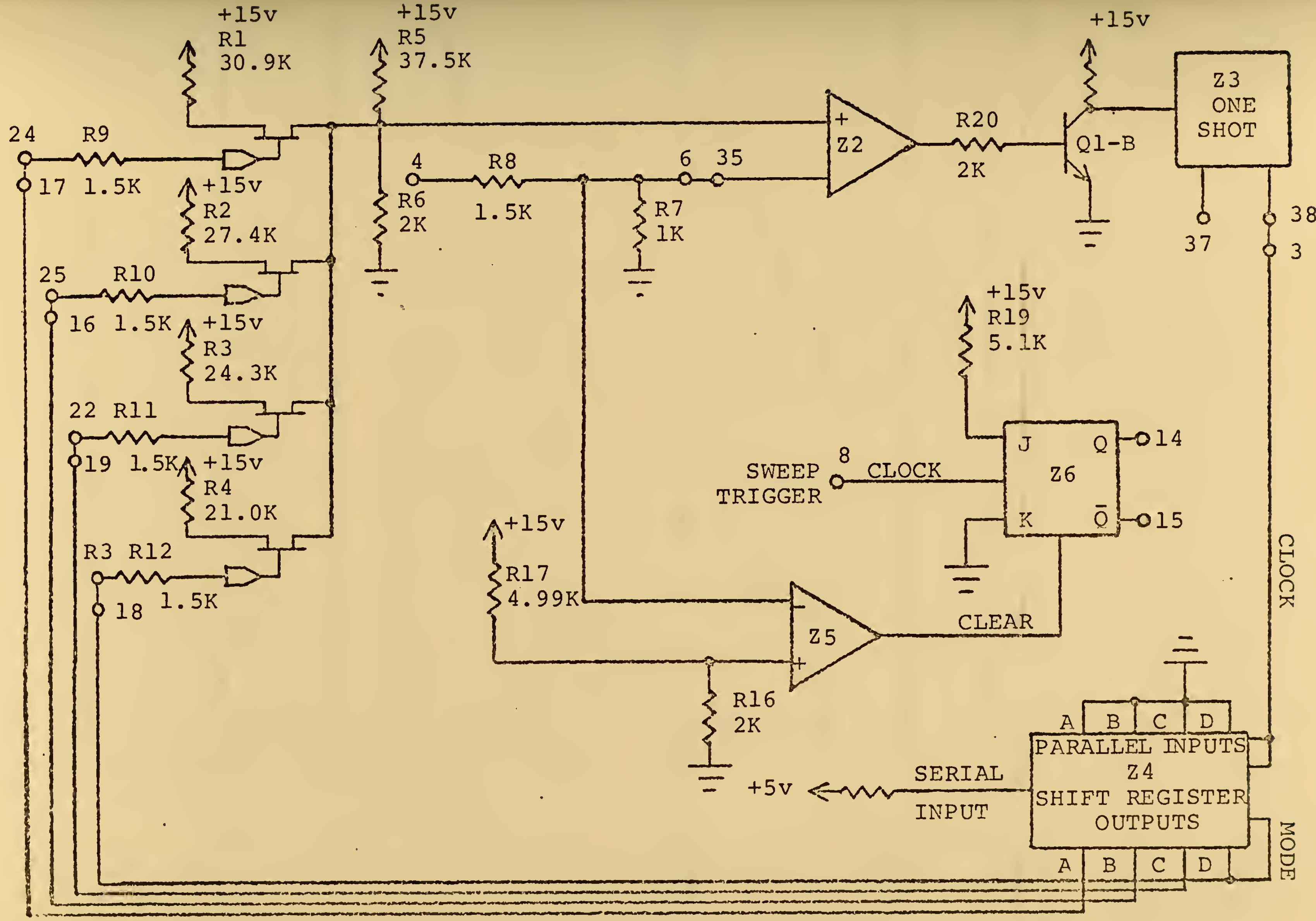


Figure 22. End Sweep Logic Block Diagram.

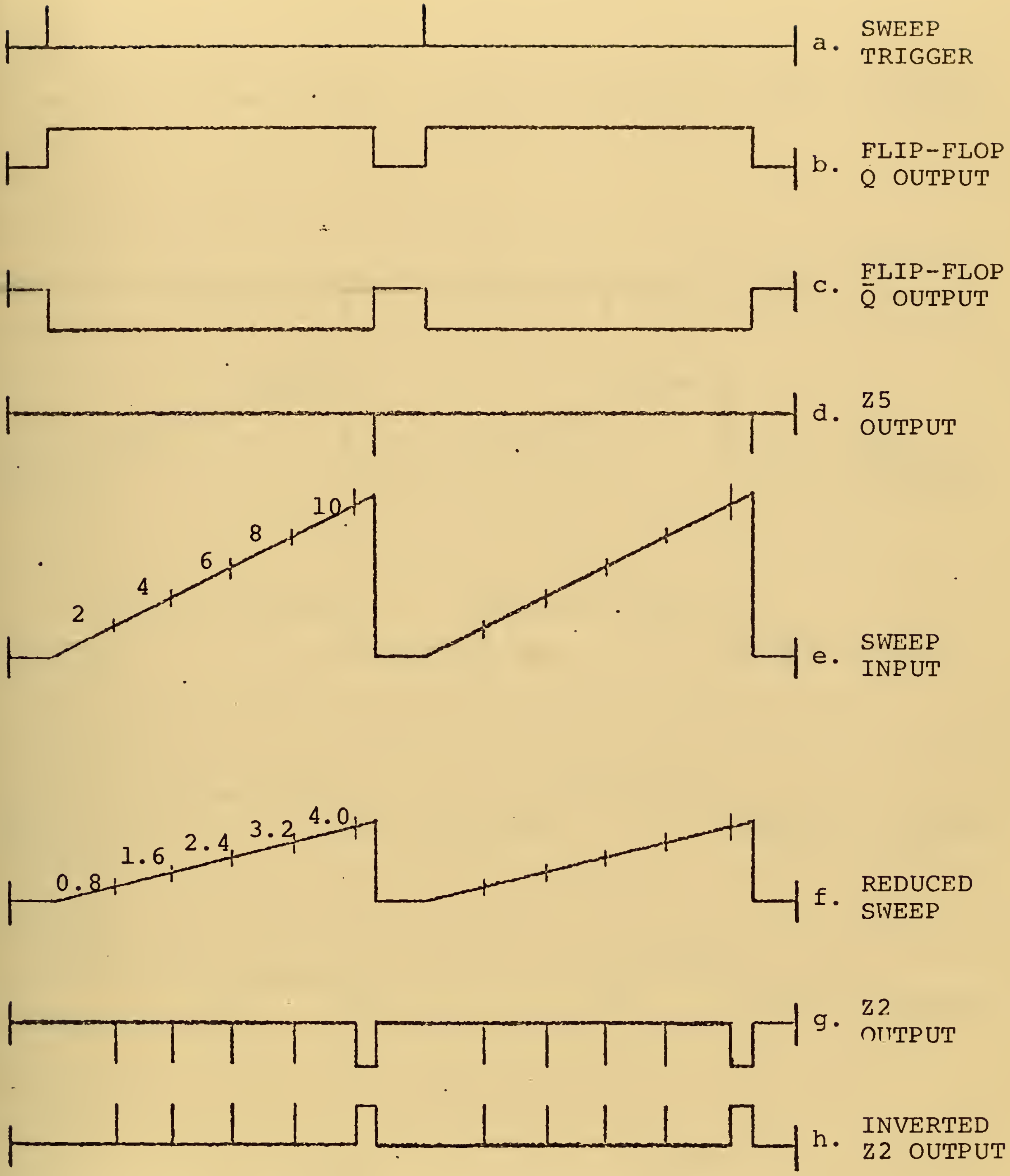


Figure 23. End Sweep Logic Waveforms.

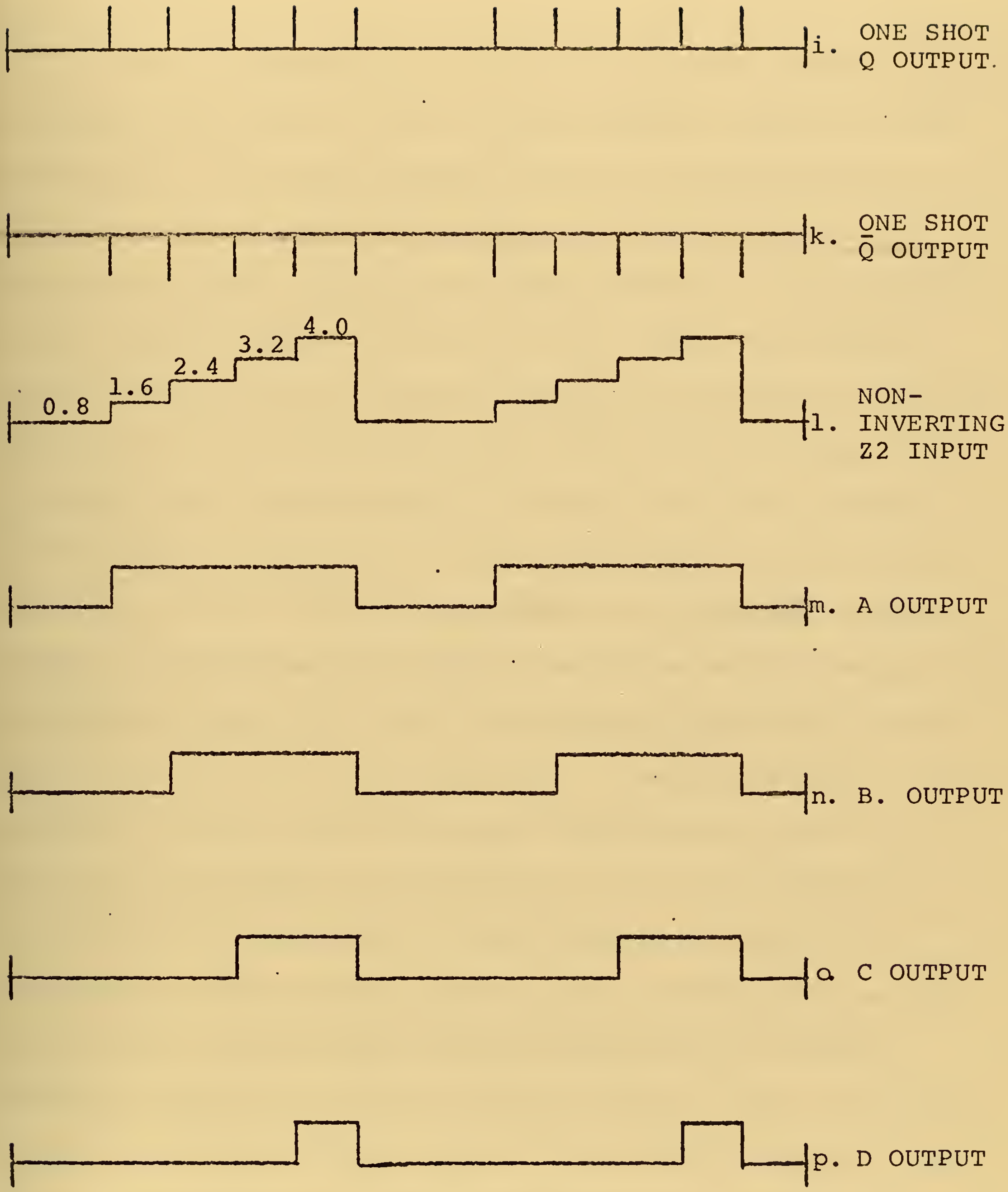


Figure 23 (Continued).

The $\bar{Q}$ output is used to stop the sweep. Another sweep trigger pulse to pin eight will cause the above process to be repeated.

Pin six is connected to pin 35 so that the reduced sweep voltage, Fig. 23(f), is fed to the inverting input of comparator Z2. The non-inverting input of comparator Z2 is connected to the resistive divider network of R5 and R6, and to the common drain of four FET switches. Resistors R5 and R6 reduce +15 volts to +0.8 volts. When the reduced sweep voltage at the inverting input of comparator Z2 becomes +0.8 volts (2.0 volts at pin four) the output of comparator Z2 goes from a logical one to a logical zero, Fig. 23(g). This signal is diverted and fed to the input of one shot Z3 as shown in Fig. 23(h). One shot Z3 is triggered by this input, a two-microsecond logical one pulse appears at pin 37 as shown in Fig. 23(i), and a two-microsecond logical zero pulse appears at pin 38, Fig. 23(k). Resistor R21 and capacitor C8 are used to set the timing of one shot Z3. Pin 38 is connected to pin three so that the $\bar{Q}$ output of one shot Z3 is connected to the clock inputs of shift register Z4. The serial input to shift register Z4 is tied to +5 volts (logical one) through resistor R15 and the parallel inputs are tied to ground (logical zero). The mode control is tied to the D output of the shift register. Initially the mode control will be logical zero which will cause the shift register to shift right serially. The clock pulse from the $\bar{Q}$ output of the one shot, Fig. 23(k), will

shift a logical one to the A output of the shift register on pin 17, Fig. 22(m). Pin 17 is connected to pin 24 so that the A output of shift register Z4 is connected to the FET driver input whose source is tied to resistor R1. A logical one at this point will turn the FET switch on and resistor R1 will be in parallel with R5. This will cause the voltage level at the non-inverting input of comparator Z2 to increase to +1.6 volts, Fig. 23(l). This will cause the output of comparator Z2 to return to a logical one, Fig. 23(g), until the reduced sweep voltage at the inverting input of comparator Z2, Fig. 23(f), becomes +1.6 volts (4.0 volts at pin four). Then the output of comparator Z2, Fig. 23(g), will be inverted as shown in Fig. 23(h), which will trigger one shot Z3. The Q output of the one shot, Fig. 23(k), will shift a logical one to the B output of shift register on pin 16, Fig. 23(n). Pin 16 is connected to pin 25 so that the B output of shift register Z4 is connected to the FET driver input whose source is tied to resistor R2. A logical one at this point will turn the FET switch on and resistor R2 will be in parallel with resistors R5 and R1. This will cause the voltage level at the non-inverting input of comparator Z2 to return to a logical one as shown in Fig. 23(g) until the reduced sweep voltage, Fig. 23(f), at the inverting input of comparator Z2 becomes +2.4 volts (6.0 volts at pin four). Then the output of comparator Z2, Fig. 23(g), will be inverted, Fig. 23(h), which will trigger one shot Z3. The $\bar{Q}$ output of the one shot, Fig. 23(k), will shift a

logical one to the C output of the shift register on pin 19, Fig. 23(o). Pin 19 is connected to pin 22 so that the C output of shift register Z4 is connected to the FET driver input whose source is tied to resistor R3. A logical one at this point will turn the FET switch on and resistor R3 will be in parallel with resistors R5, R1, and R2. This will cause the voltage level at the non-inverting input of comparator Z2 to increase to +3.2 volts, Fig. 23(l). This will cause the output of comparator Z2 to return to a logical one, Fig. 23(g), until the reduced sweep voltage, Fig. 23(f), at the inverting input of comparator Z2 becomes +3.2 volts (8.0 volts at pin four). Then the output of comparator Z2, Fig. 23(g), will be inverted, Fig. 23(h), which will trigger one shot Z3. The $\bar{Q}$ output of the one shot, Fig. 23(k), will shift a logical one to the D output of the shift register on pin 18, Fig. 23(p). The mode control of the shift register is connected to the D output. Pin 18 is connected to pin 23 so that the D output of shift register Z4 is connected to the FET driver input whose source is tied to resistor R4. A logical one at this point will turn the FET switch on and resistor R4 will be in parallel with resistors R5, R1, R2 and R3. This will cause the voltage level at the non-inverting input of comparator Z2 to increase to +4.0 volts, Fig. 23(l). In turn the output of comparator Z2 is returned to a logical one, Fig. 23(g), until the reduced sweep voltage at the inverting input of comparator Z2, Fig. 23(f), becomes +4.0 volts (10.0 volts at pin four).

Then the output of comparator Z2, Fig. 23(g), is inverted, Fig. 23(h), and this triggers one shot Z3. Since the mode control of the shift register is now a logical one, the $\bar{Q}$ output of the one shot, Fig. 23(k), shifts a logical zero to all the shift register outputs. This causes the voltage level at the non-inverting input of comparator Z2 to decrease to +0.8 volts, Fig. 23(l). The output of comparator Z2 then returns to a logical one when the sweep input returns to zero. Another sweep on pin four will cause the above process to be repeated.

APPENDIX H

INTEGRATOR (MODULE B4)

The integrator module was built by NAFI for use in several systems. When a DC voltage is applied at the input, the integrator will provide a linear ramp output voltage with a slope which can be varied by selecting one of five different combinations of input resistance, only four of which are used in this application. The following description was, for the most part, extracted from Ref. 1.

Side A of the module utilizes a Siliconix DG123L 5-channel driver with FET switches and a Harris Semiconductor HA-2600 high-impedance op amp. Side B uses a Siliconix DG133L 2-channel driver with SPST FET switches. The circuit diagrams for sides A and B are shown in Fig. 24 and 25. C1, C2, C3, C6 and C7 are used as decoupling capacitors for the ±15 volt and +5 volt supplies.

Figure 26 may be examined in conjunction with the following discussion for an understanding of how the integrator module performs its function. A DC level applied to pins 19 and 15 will be integrated according to the equation

$$E_o = - \frac{1}{R_i C_5} \int E_i \, dt. \qquad (7)$$

Five FET switches control the value of the input resistance. Either R4, R5, R6, R7 or R8 is used as the input resistance. An integrator results by using C5 as a feedback capacitor

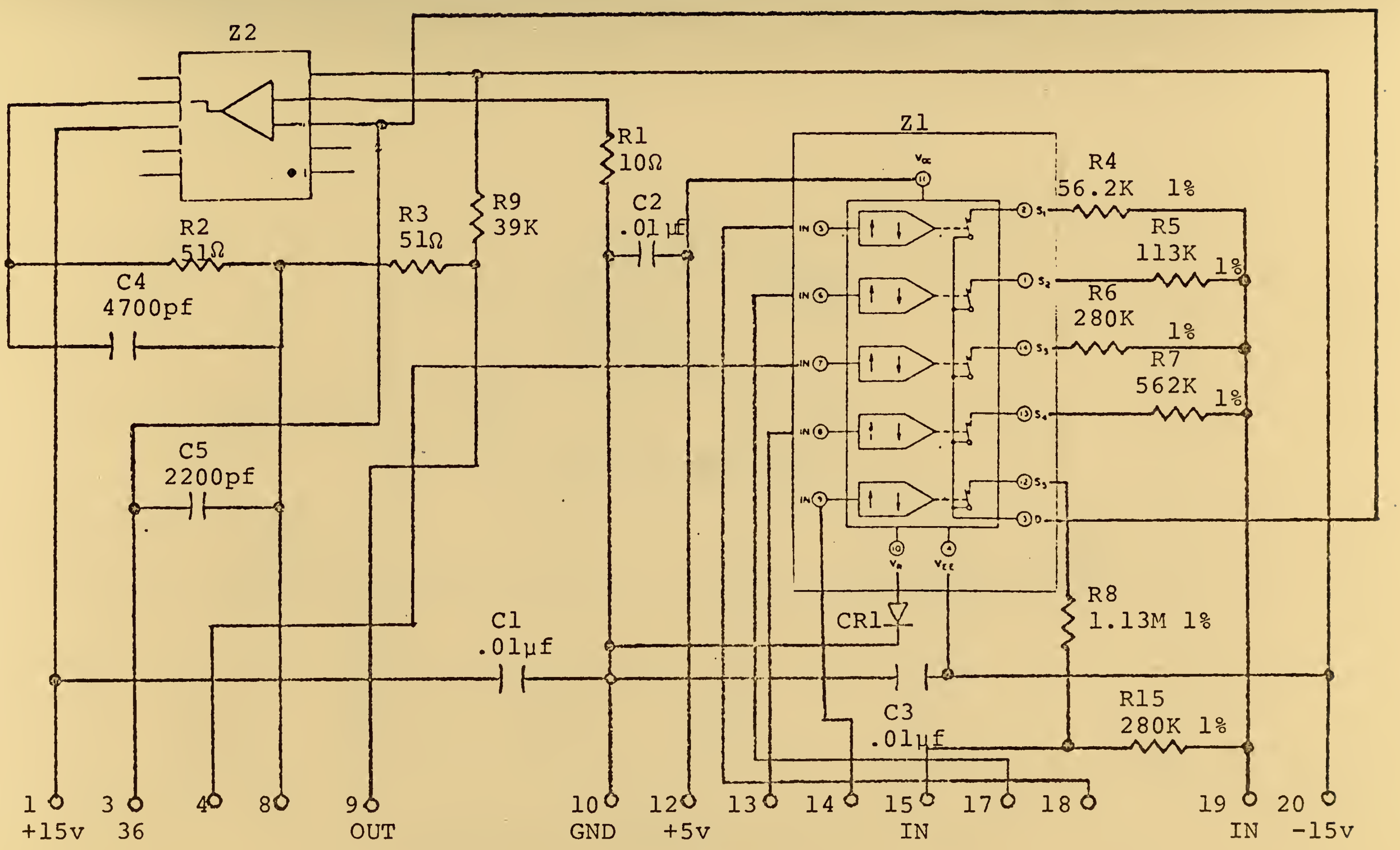


Figure 24. Integrator Module - Side A.

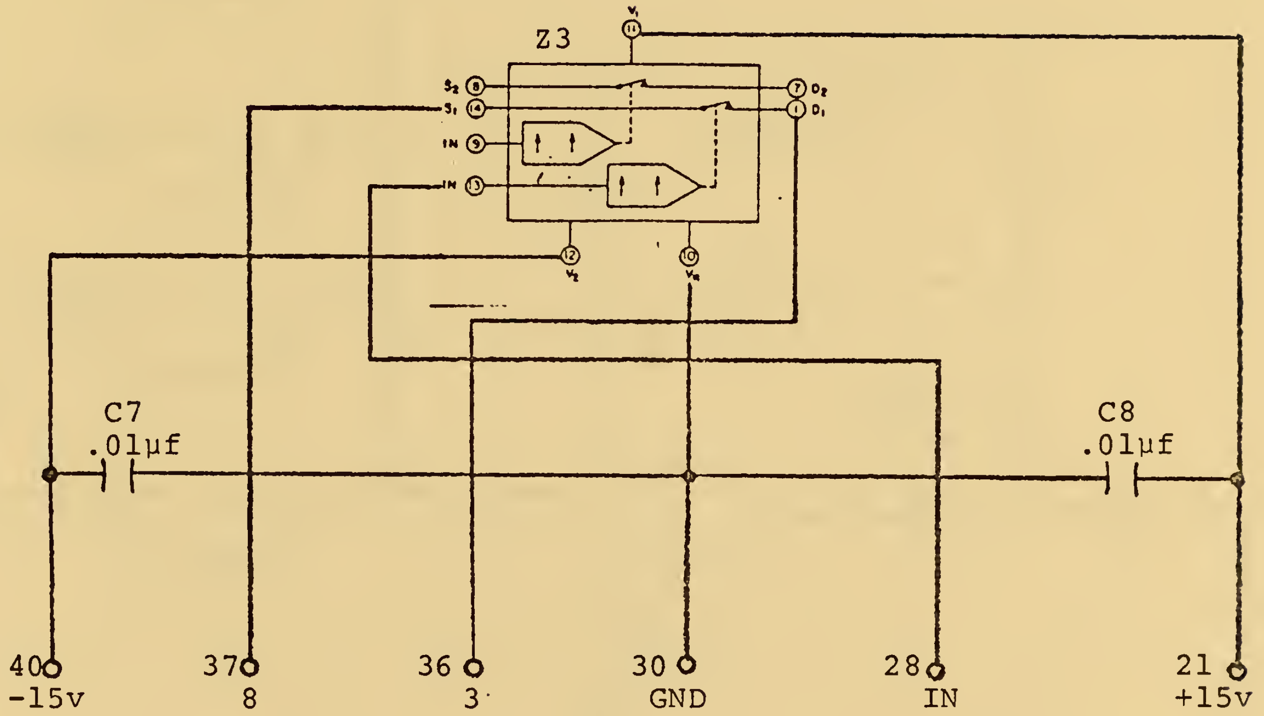


Figure 25. Integrator Module - Side B.

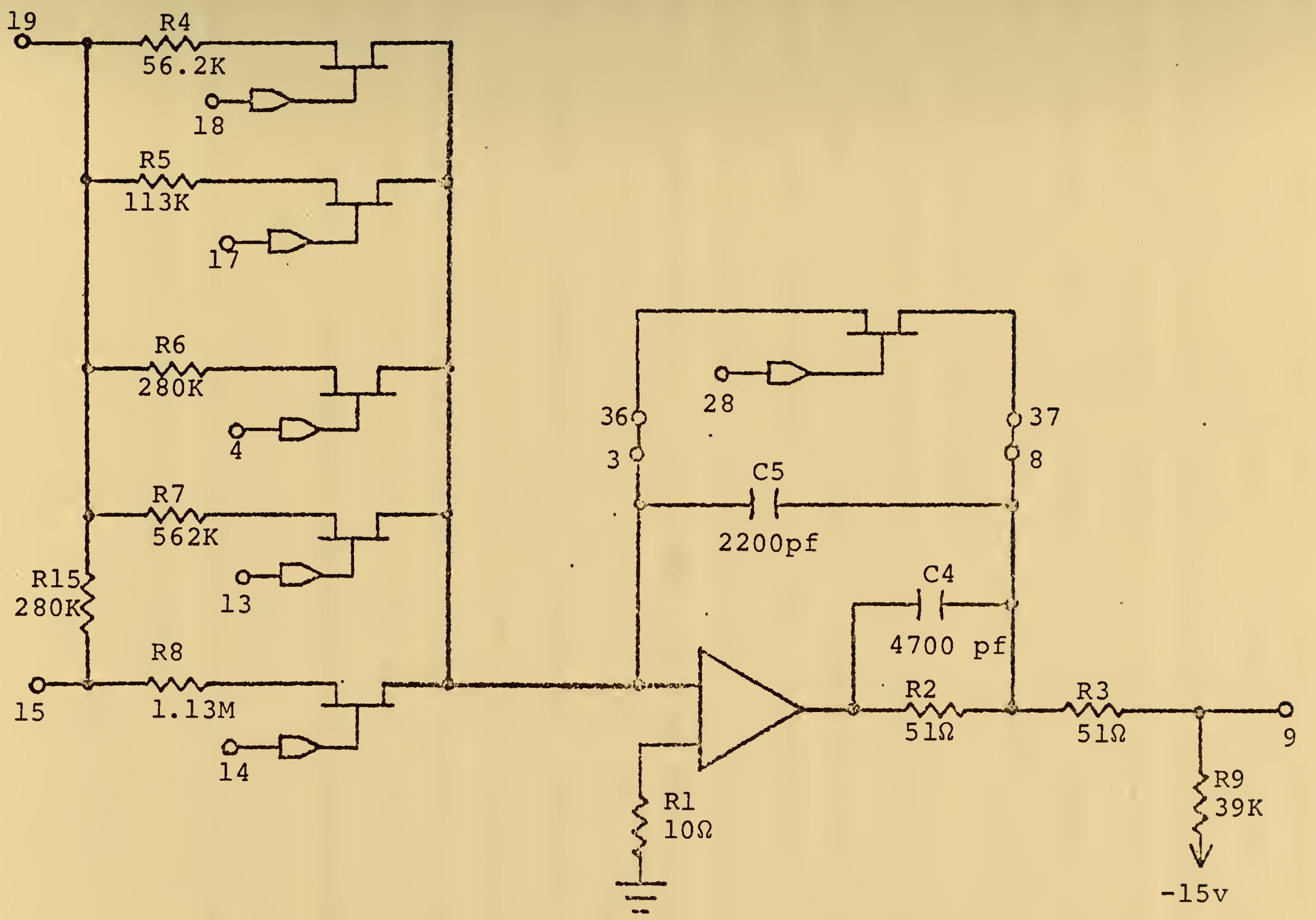


Figure 26. Integrator Block Diagram.

for op amp Z2. For normal operation a FET switch from side B is connected across the feedback capacitor as a reset switch. Resistor R2 provides short-circuit protection and capacitor C4 adds stabilization. Resistors R3 and R9 provide a biasing network of approximately -20 millivolts to compensate for the offset produced by the FET switch across the feedback. Diode CR1 from pin 10 of Z1 to ground increases the input switching threshold voltage to approximately +1.5 volts and improves noise immunity.

The following is an example of the operation of the integrator. A -10 volt DC level is applied to pins 15 and 19 and the FET switch across the feedback capacitor is turned on. The output of the integrator is then zero. Assume the FET switch in series with R6, the 100 nautical mile range scale, is turned on, and the FET switch across the feedback is turned off by a logical zero level from the end-sweep-logic module at pin 28. The output increases linearly until the end-sweep-logic module detects a sweep amplitude of +10 volts at pin 9. Then the logic level at pin 28 is changed to a logical one which turns on the FET switch and allows the integrating capacitor to discharge. The integrator will remain idle until a logic level change at pin 28 allows it to repeat the process.

APPENDIX I

INVERTER AND BUFFER AMPLIFIERS (MODULE B5)

This module was designed by the author. It utilizes four HA-2600 op amps. Two of the op amps are configured as inverters and the other two as buffers.

Side A, Fig. 27, contains two inverting amplifier circuits whose components serve the following functions. Input resistor R3 and feedback resistor R4 set the gain of the inverting input of op amp Z1 and unity. The non-inverting input of Z1 is held at ground through resistor R8. The sweep voltage, R_a, from integrator module pin nine is fed into the module at pin 12, inverted with unity gain through Z1 and fed out at pin 18. Input resistors R1 and R5 and feedback resistor R2 set the gain of the inverting inputs of op amp Z2 at unity for the input which is connected to the output of Z1 and approximately 0.01 for the input at pin 13, which provides an offset voltage from potentiometer R9 of module B6. The voltage-divider network of R6 and R7 in conjunction with the non-inverting gain of Z2, as determined by R1, R2 and R5, set the non-inverting gain between the input at pin six, which is the $\bar{Q}$ output of one shot Z6 on the end-sweep-logic module, and the output of Z2 at 0.4. C1 and C2 are decoupling capacitors for the ±15 volt DC supplies.

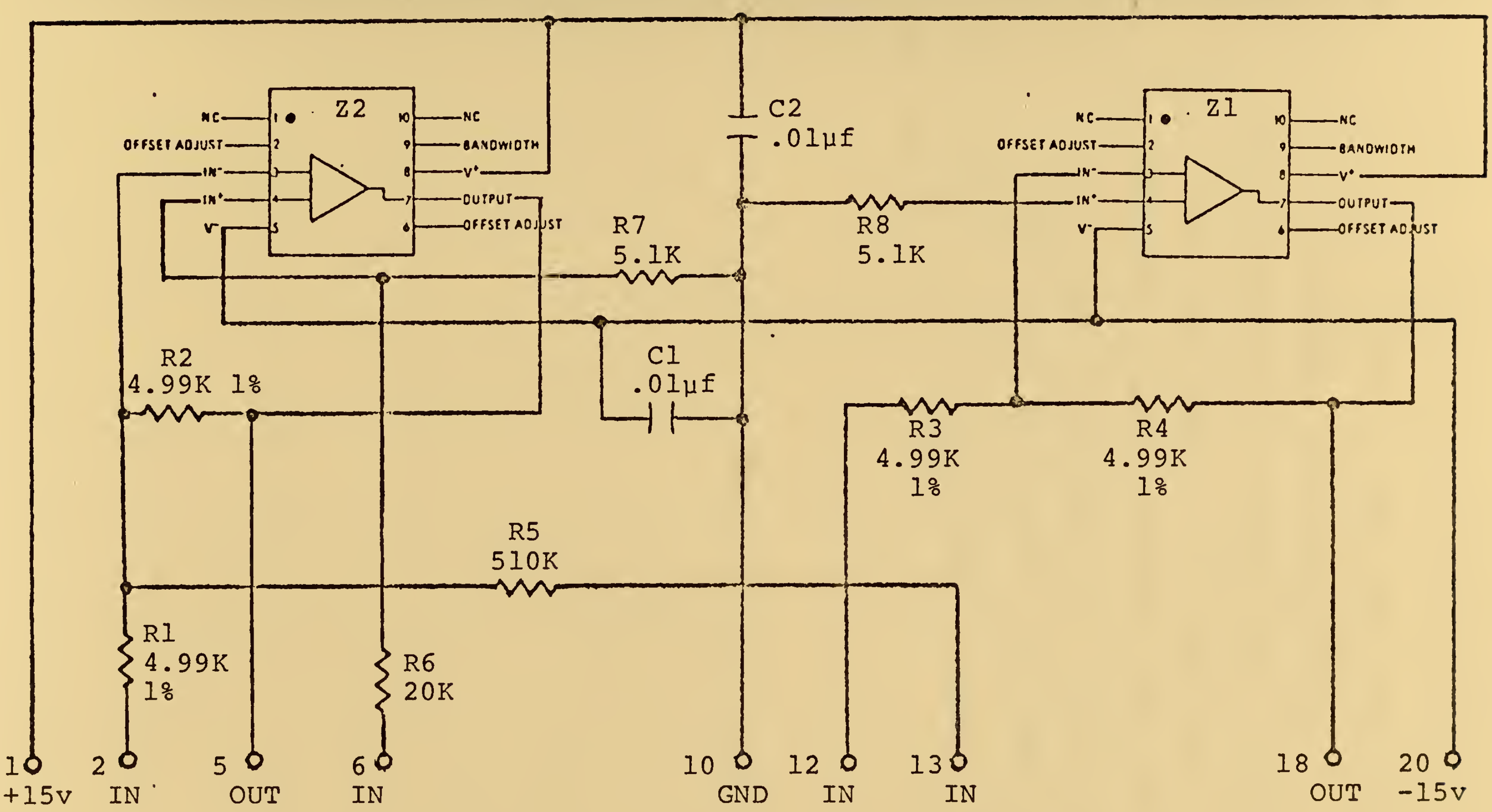


Figure 27. Inverter and Buffer Amplifiers Module - Side A.

Side B, Fig. 28, contains two buffer-amplifier circuits. The two circuits are identical voltage followers with R9 and R10 tying the inverting inputs to ground and C3 and C4 decoupling the ±15 volt supplies. The input to Z3, $y = R \cos \phi$, comes to pin 37 of the module from the cosine output of the sin/cos potentiometer. The output goes to the Y output on the rear panel of the processor, and to the input of one of the inverters on module B6. The input to Z4, $x = R \sin \phi$, comes to pin 26 from the sine output of the sin/cos potentiometer, and the output goes to the X output on the rear panel.

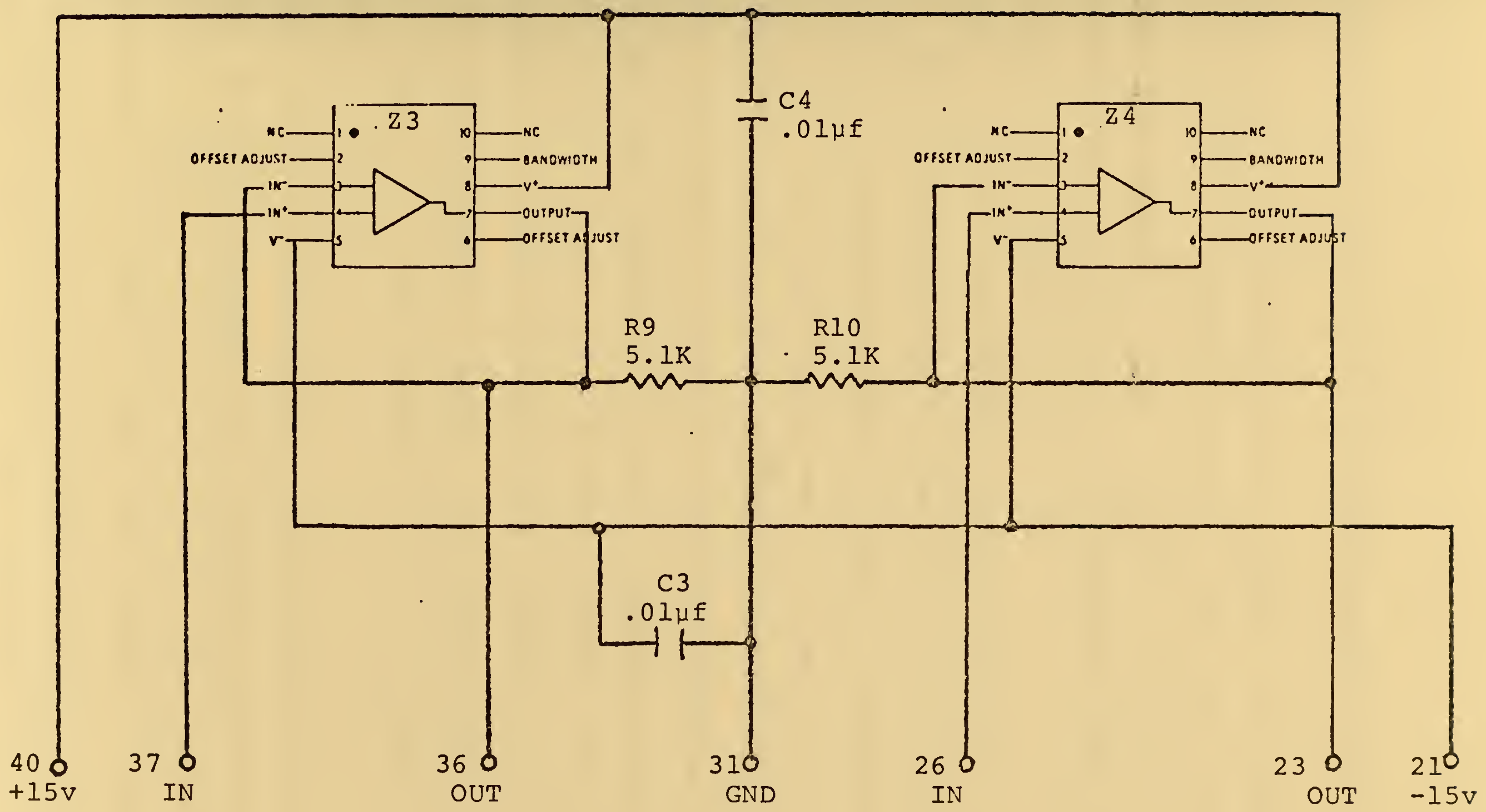


Figure 28. Inverter and Buffer Amplifiers Module - Side B.

APPENDIX J

INVERTER AMPLIFIER AND POTENTIOMETER ADJUST (MODULE B6)

This module was designed by the author. It utilizes two HA-2600 op amps as inverters on side A, Fig. 29, and two 10K potentiometers on side B, one to provide -10 volts DC to the integrator module and the other to provide an offset voltage to inverter Z2 on module B5, Fig. 30.

Side A contains two identical inverter-amplifier circuits. Resistors R1 and R2 set the gain of the inverting input of Z1 at unity as do R3 and R4 for Z2. Resistors R5 and R6 tie the non-inverting inputs of Z1 and Z2 to ground. Capacitors C1 and C2 provide decoupling for the 15 volt DC supplies. The input to inverter Z1 comes to pin two of the module from the Y output, $y = R \cos \phi$, buffer on module B5. Its output goes to the range correction module. The input to inverter Z2 is the corrected sweep voltage R_c which comes from the range correction module. Its output goes to the range correction (In-Out) switch on the front panel of the processor.

Side B contains two circuits. In the first circuit resistor R7 and the 12-volt zener diode CR1 are used to reduce the -15 volt supply to -12 volts. Then the 10K potentiometer R8 is used to pick off a variable voltage of from zero to -12 volts DC from across the zener. This circuit provides the -10 volt DC level required by the

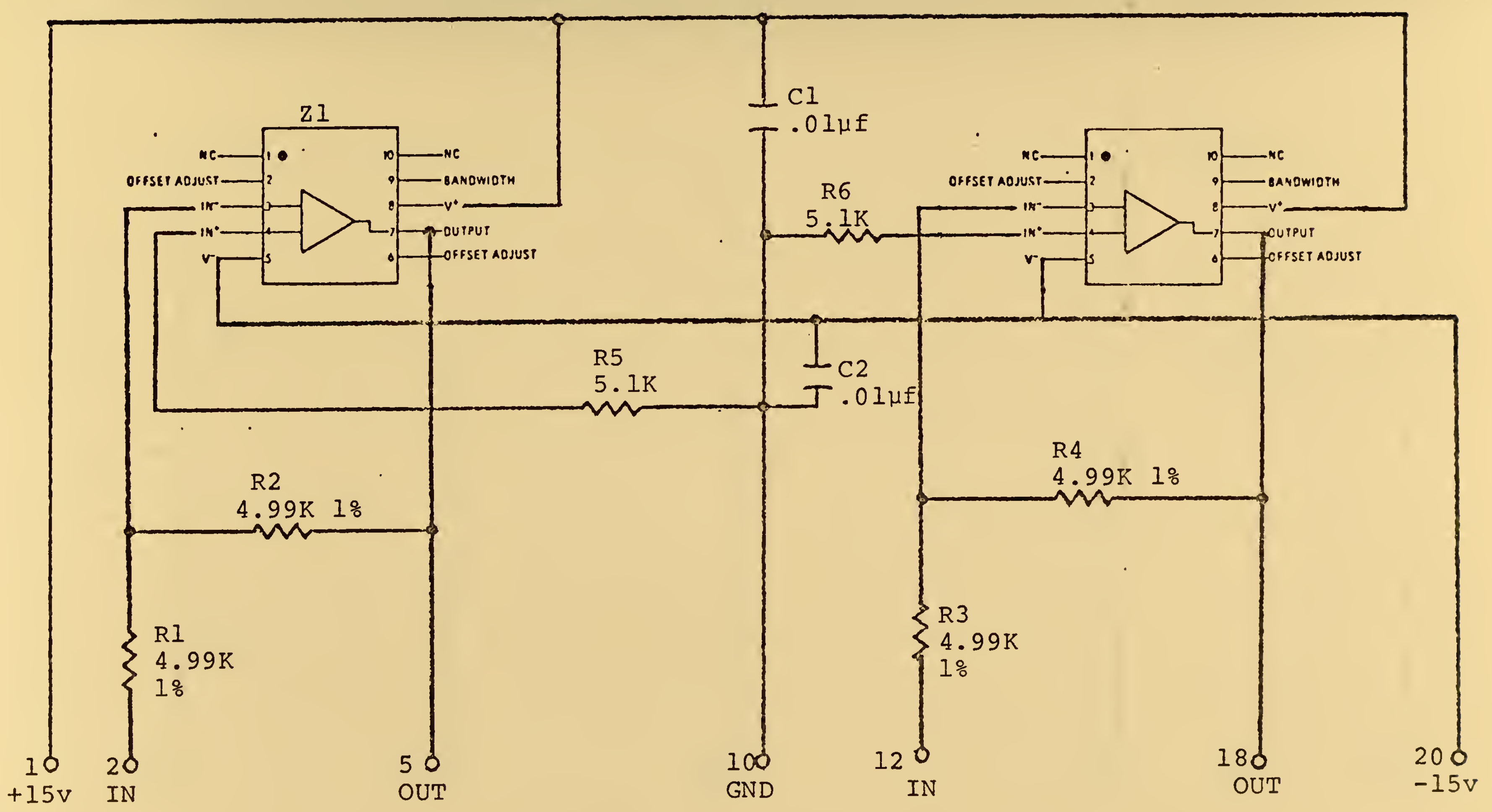


Figure 29. Inverter Amplifier and Potentiometer Adjust Module - Side A.

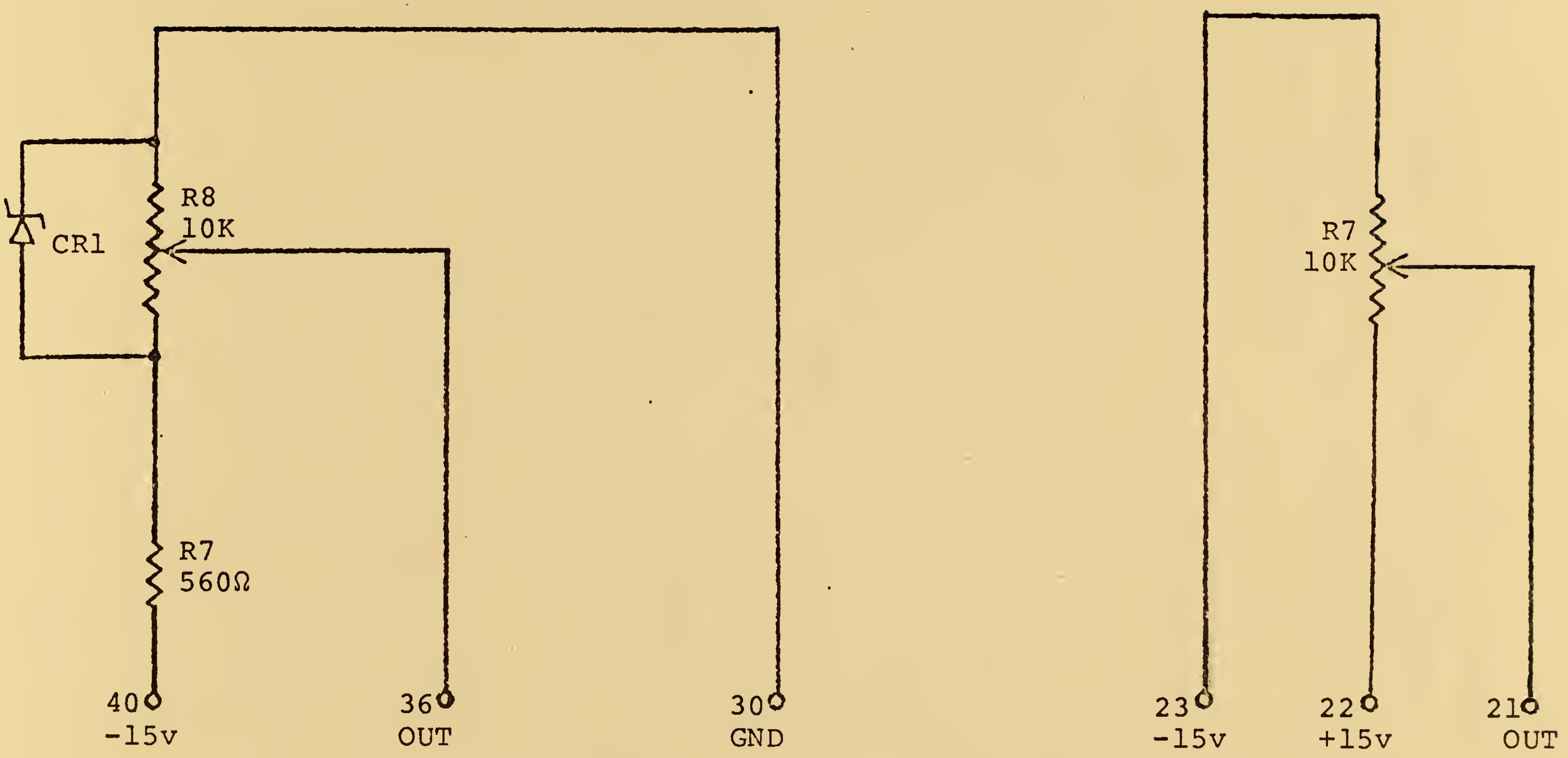


Figure 30. Inverter Amplifier and Potentiometer Adjust Module - Side B.

integrator module. The second circuit is the 10K potentiometer R9 with +15 volts DC tied to one terminal and -15 volts DC tied to the other terminal so that a variable voltage of from -15 volts to +15 volts is available at the wiper for use as the offset voltage input for one of the inverter amplifiers on module B5.

APPENDIX K

VIDEO SUMMING AMPLIFIER (MODULE B7)

This module is a two-stage video summing amplifier which was designed by the author to provide the Z input to the PPI display unit. It is a "picture frame" module. This means that the center of the module is cut out in the same manner as a picture frame, and the extra space obtained allows thicker components to be used. Use of this type module was necessary because the two HA-2700 op amps utilized were not readily available in the flatpack configuration. The TO-99 cans, which were used, are too large for the normal two-sided module used elsewhere in the system.

The two-stage video summing amplifier circuit, Figure 31, functions in the following manner. Resistors R1 through R5 are input resistors for the five inputs to Z1. The output of Z1 is the sum of the five inputs with their respective gains as indicated by each input resistance in conjunction with the feedback resistor R6. This output is fed out of the module at pin 36 and is also fed into Z2 through input resistor R7. Resistor R8 is the feedback resistor for Z2. The output of Z1 is inverted with unity gain by Z2 and fed out of the module at pin 33.

Figure 32 depicts the module with its inputs. The intensity input to pin 23 of the module is controlled by the intensity knob on the front panel of the processor. This knob

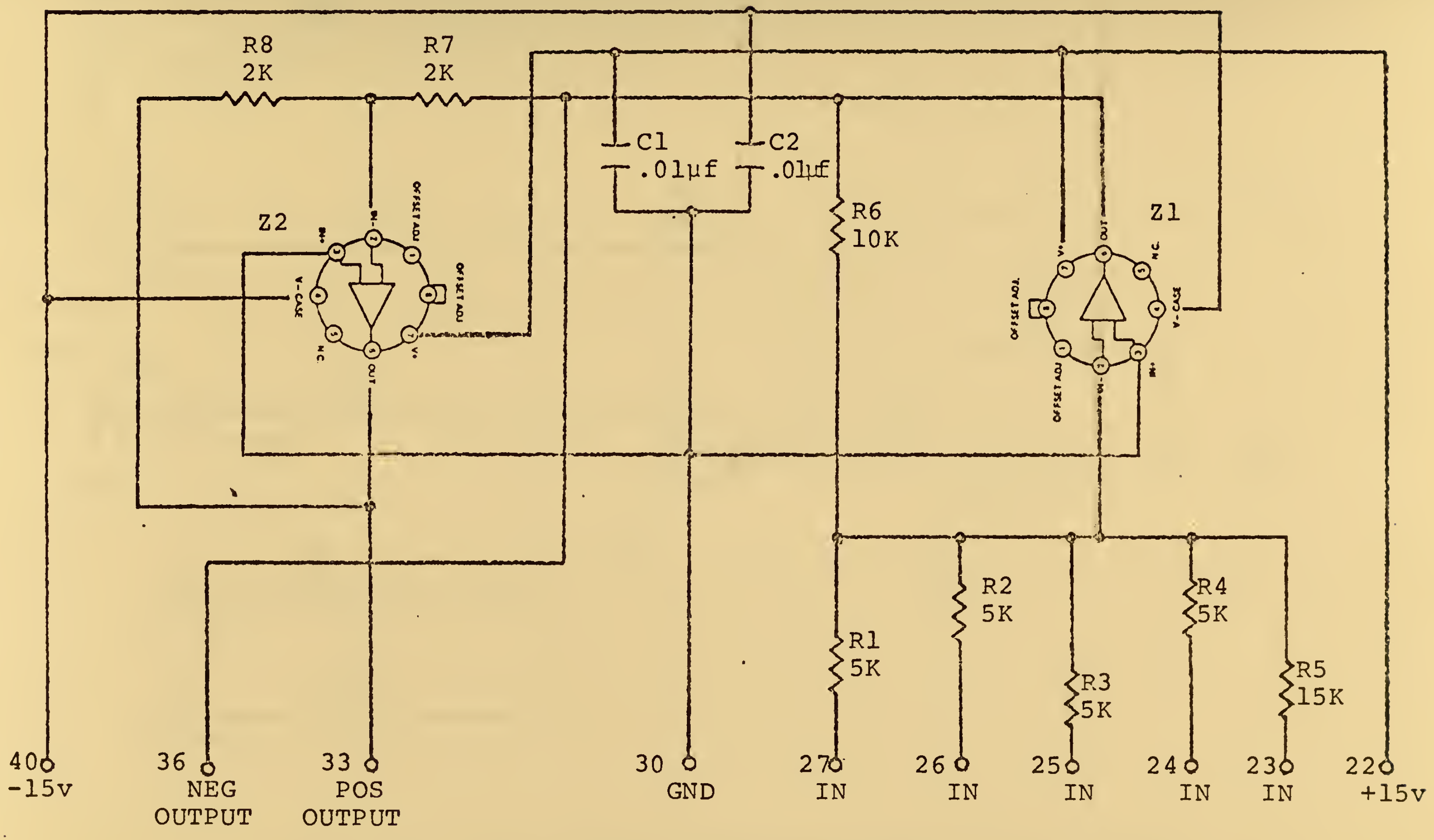


Figure 31. Video Summing Amplifier.

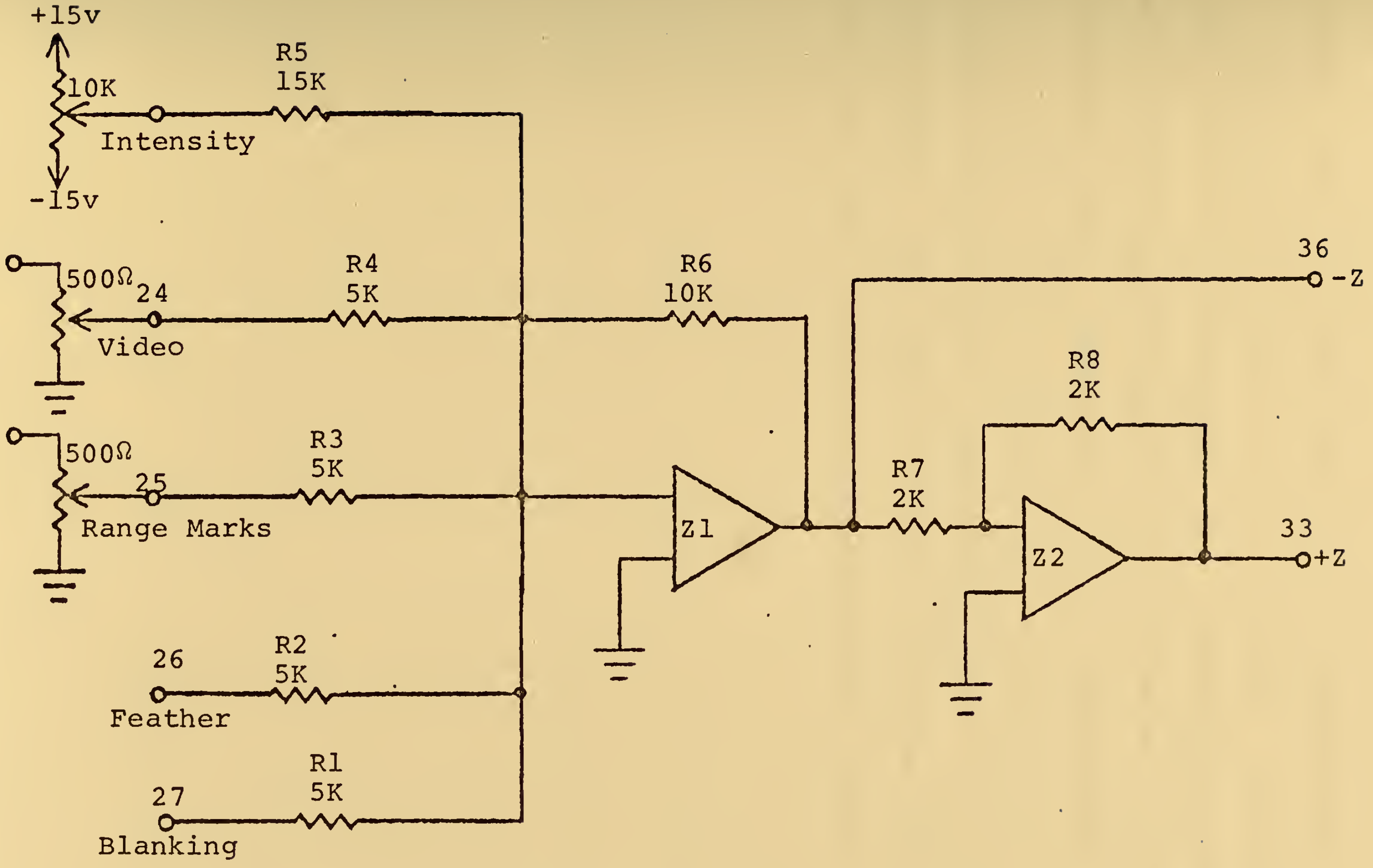


Figure 32. Video Summing Amplifier Module Block Diagram.

adjusts the wiper of a 10K potentiometer to a setting of from -15 volts to +15 volts. The video input to pin 24 of the module comes from the video input on the rear panel through a 500-ohm potentiometer. The potentiometer output is controlled by a knob on the front panel. The range marks input to pin 25 of the module comes from the end-sweep-logic module through a 500-ohm potentiometer whose output is controlled by a knob on the front panel. The feather input to pin 26 comes from the feather-logic module pin six. The blanking input to pin 27 comes from pin 14 of the end-sweep-logic module. The output of Z1 is a negative video signal while the output of Z2 is a positive video signal.

APPENDIX L

RANGE CORRECTION (MODULE B8 AND B9)

This module was built by the author as a modification of NAFI's multiply-and-divide module. Its function is to generate an electronic solution to the bistatic radar range correction problem. Side A, Fig. 33, utilizes two HA-2600 op amps and one GPS Corporation hybrid 4-quadrant multiplier. The multiplier gives an instantaneous output which is one tenth the product of the two input voltages. The hybrid multipliers packaging requires the module to take up the space normally reserved for two modules. Side B, Fig. 34, of the module contains two 10K potentiometers, which are used to provide offset voltages to the two op amps on side A.

On side A of the module, Z2 is configured as a summing amplifier with R1, R2 and R3 as input resistors and R4 as the feedback resistor. Resistor R5 ties the non-inverting input to ground. Resistors R6 and R7 in conjunction with capacitors C1 and C2 low-pass filter the ±15 volt DC supplies. Resistors R8 and R9 with capacitors C3 and C4 low-pass filter the two inputs to multiplier Z1. R10, R11 and R12 are input resistors to inverter Z3 while R13 is the feedback resistor. Resistor R14 ties the non-inverting input to ground.

Side B consists of two identical 10K potentiometers R15 and R16 with +15 volts tied to one terminal and -15 volts

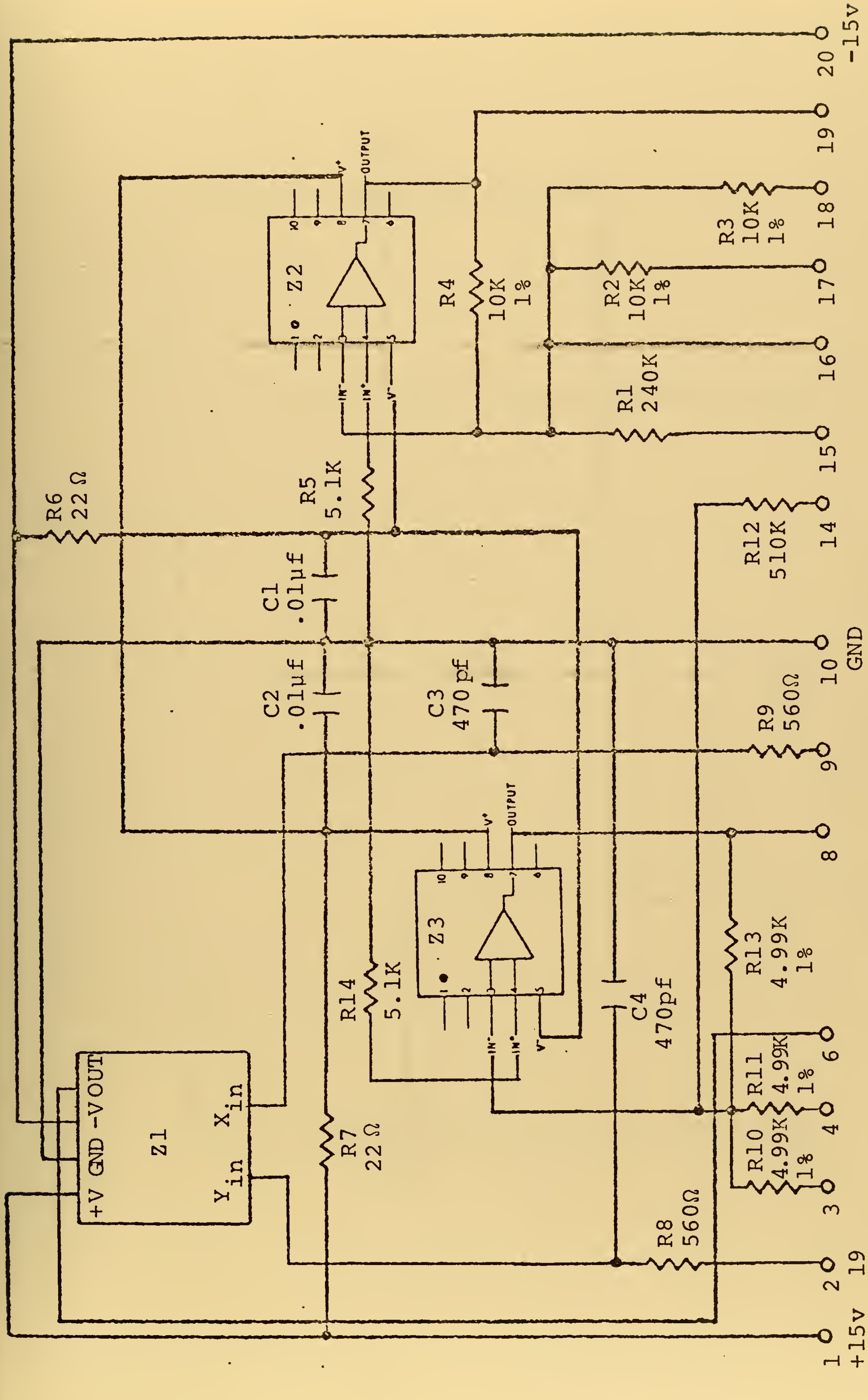


Figure 33. Range Correction Module - Side A.

Figure 34. Range Correction Module - Side B.

tied to the other terminal. This provides a variable voltage of from -15 volts to +15 volts at the wiper of each potentiometer. These circuits are used to provide offset voltages to the two op amps on side A of the module.

Figure 35 shows a diagram of both sides of the module with their interconnections. As shown in section I.B, the equation for the corrected bistatic radar range is

$$R_c = R_a + \frac{D(R_a - y)}{R_a + D} = R_a + z. \qquad (8)$$

The equation is implemented on the module in the following manner. Positive R_a from inverter Z2 of module B5 is fed to the module at pin nine and tied to the X input to multiplier Z1. Positive R_a from the integrator module is fed to the module at pin 17 and tied to the inverting input of Z2 through R13. Negative y from inverter Z1 of module B6 is fed to the module at pin 18 and tied to the inverting input of Z2 through R2. The output of the multiplier Z1 is routed through pin six of the module to the estimated range potentiometer (D) on the processors front panel and back to pin 16 of the module which is tied to the inverting input of Z2. The output of Z2, pin 19 of the module, is tied back to the Y input to the multiplier through pin 2 of the module.

A simple analysis of the circuit of Z2 will show that the output at pin 19 is indeed that given for z in the equation above. The output of the multiplier is one tenth the product of its two inputs and the contribution of an input voltage

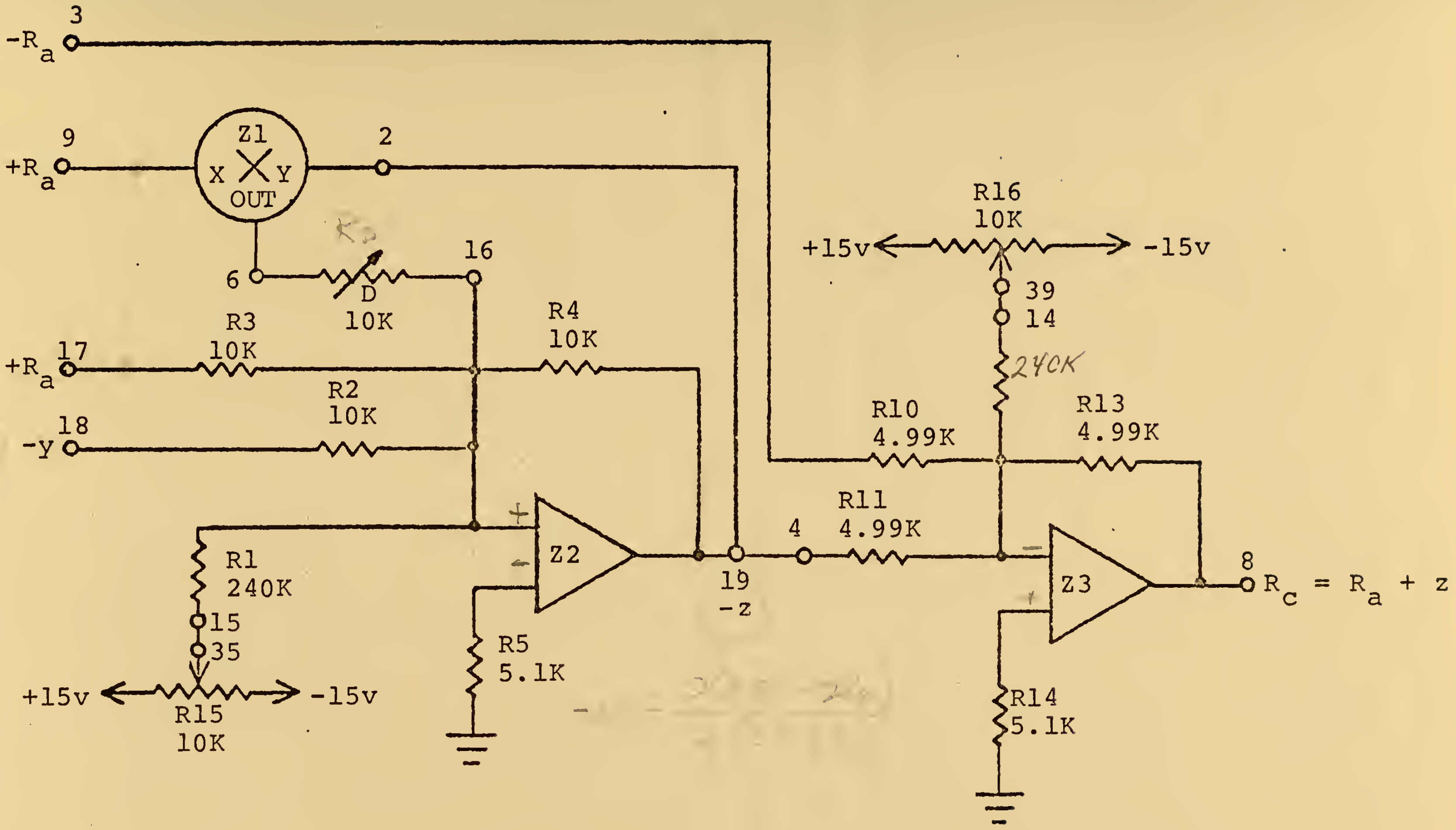


Figure 35. Range Correction Module Block Diagram.

to an inverting amplifier is the feedback resistance divided by the input resistance times the negative of the input voltage. Thus the equation for the output of Z2 is

$$-z = -\frac{(-z)R_a(10)}{10D} - \frac{10R_a}{10} + \frac{10y}{10} \tag{9}$$

which yields

$$z = \frac{D(R_a - y)}{R_a + D}, \quad \text{Q.E.D.} \tag{10}$$

Negative R_a from invertor Z1 of module B5 is fed into the module and tied to the inverting input of Z3 along with the -z output of Z2. The output of Z3 at pin eight of the module is $+R_c$. This, of course, is the corrected sweep voltage which represents the corrected bistatic radar range.

APPENDIX M

FEATHER LOGIC AND PULSE STRETCHER (MODULE B10)

This module was built by the author. Side A is identical to side A of NAFI's feather logic module which they built for their bistatic radar processor, Ref. 1. The circuit is designed to determine when the main lobe of a radar is being received and to generate a pulse, which will produce a feather on the PPI, during the time that a main lobe is being detected. Side B is a circuit designed to stretch or increase the pulse duration of video pulses applied to the circuit.

Side A, Fig. 36, contains three Texas Instruments integrated circuits. Z1, Z2 and Z3 respectively are a SN5400 quadruple 2-input positive NAND gate, a SN5473 dual J-K master-slave flip-flop and an SN5495 4-bit right-shift left-shift register. R1 and R2 tie the J inputs of the two flip-flops on Z2 to +5 volts (logical one). The K inputs of both flip-flops are tied to ground (logical zero). R3 ties the right-shift serial input to +5 volts (logical one). The left-shift serial input is tied to ground (logical zero). C1 provides decoupling for the +5 volt supply.

Side B, Fig. 37, contains a dual NPN transistor, only one of which is used. C2 acts as a DC block. C3 is a decoupling capacitor for the +5 volt supply. R4 and R5 provide biasing for the transistor. R6 is a current limiter for the collector circuit. C4 and R7 provide an RC time

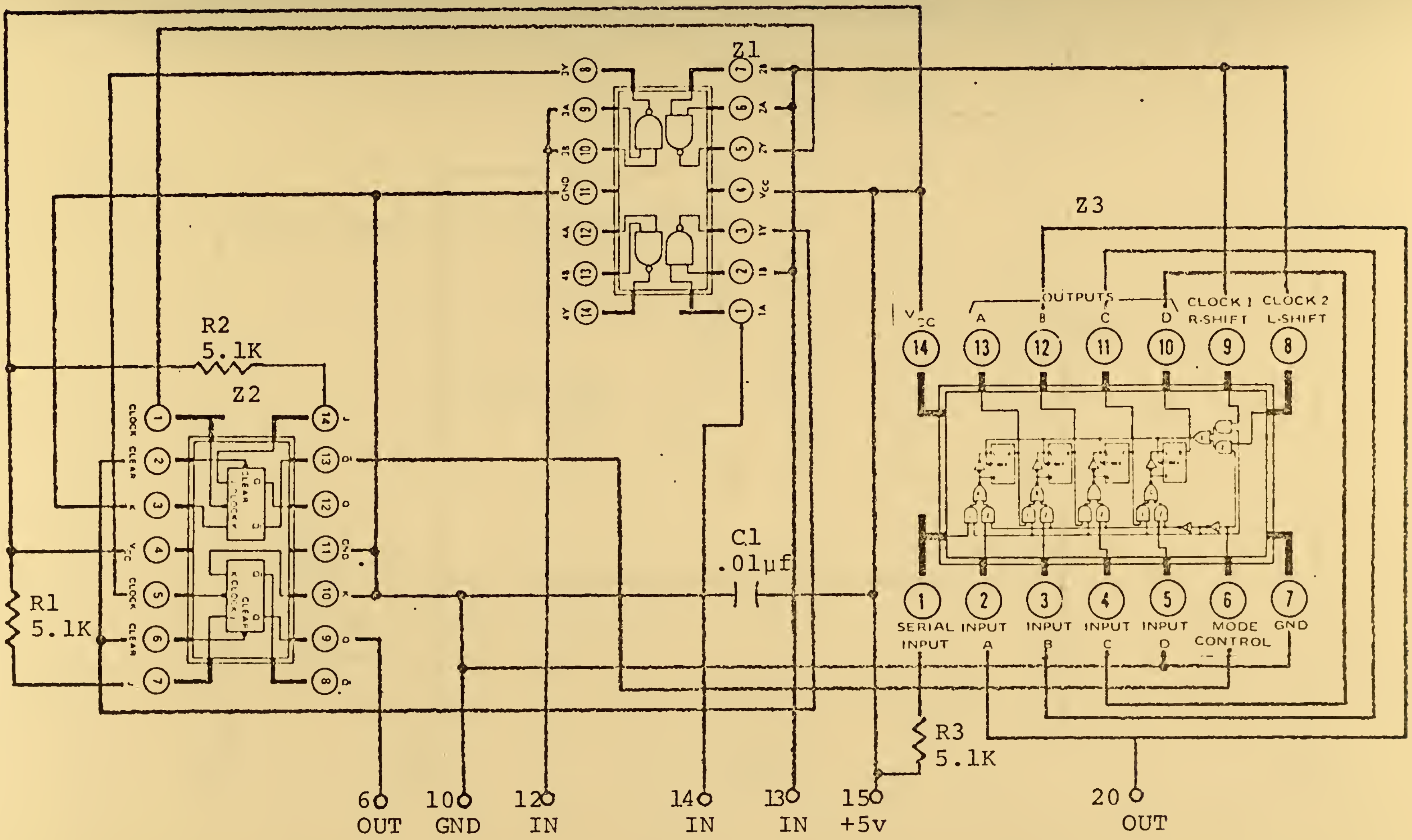


Figure 36. Feather Logic and Pulse Stretcher Module - Side A.

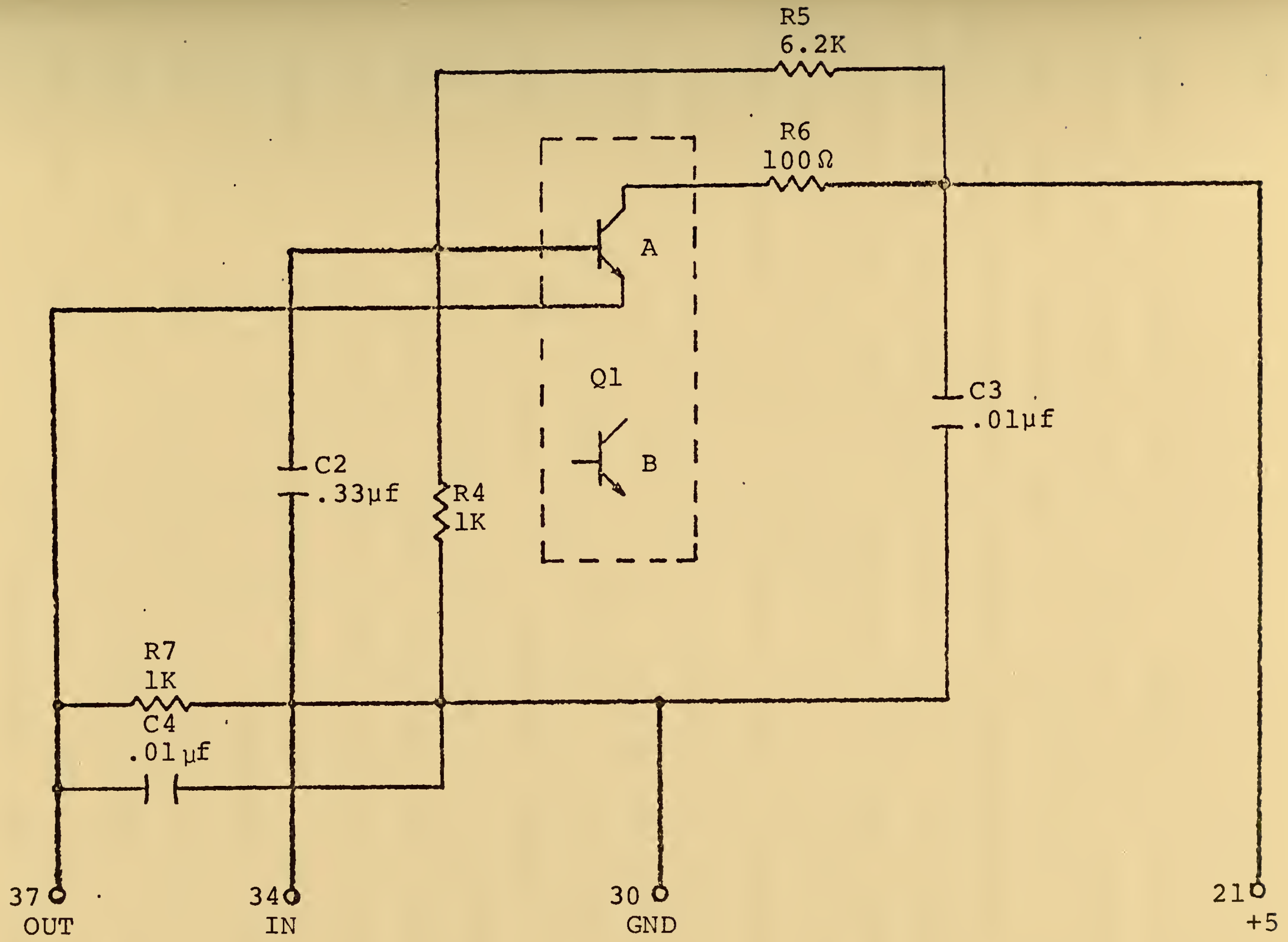


Figure 37. Feather Logic and Pulse Stretcher Module - Side B.

delay of sufficient length to increase the width of incoming pulses.

The following description of how side A performs its function was extracted from Ref. 1. Refer to Fig. 38 for a block diagram of the circuit. With pin 14 at a logical zero, logical one pulses applied to pin 13 from the one microsecond one shot on module B2 are inverted through NAND gate three and clock flip-flop two (FF-2). This causes the $\bar{Q}$ output of FF-2, which is connected to the mode control of shift-register Z3, to be a logical zero. A logical zero at the mode control of shift-register Z3 causes right-shift and a logical one causes left-shift. Since pin 13 is also connected to the clock inputs of Z3, a logical one is shifted to output A, then output B, then output C, and finally output D of Z3. Since output D is connected to input C, output C is connected to input B, and output B is connected to input A of Z3, inputs A, B and C of Z3 are then logical one. If a logical one pulse applied to pin 14 from the threshold detector on module B11 is synchronized with a logical one pulse applied to pin 13, the output of NAND gate 2 clears FF-2. This causes the mode control of Z3 to become a logical one, and a logical zero is shifted to output D which is connected to input C of Z3. If three logical one pulses in a row at pins 13 and 14 are synchronized, input A of Z3 (pin 20) becomes a logical zero. Normally four or more synchronized logical one pulses in a row appear at pins 13 and 14 from the main lobe of a radar. This insures all four

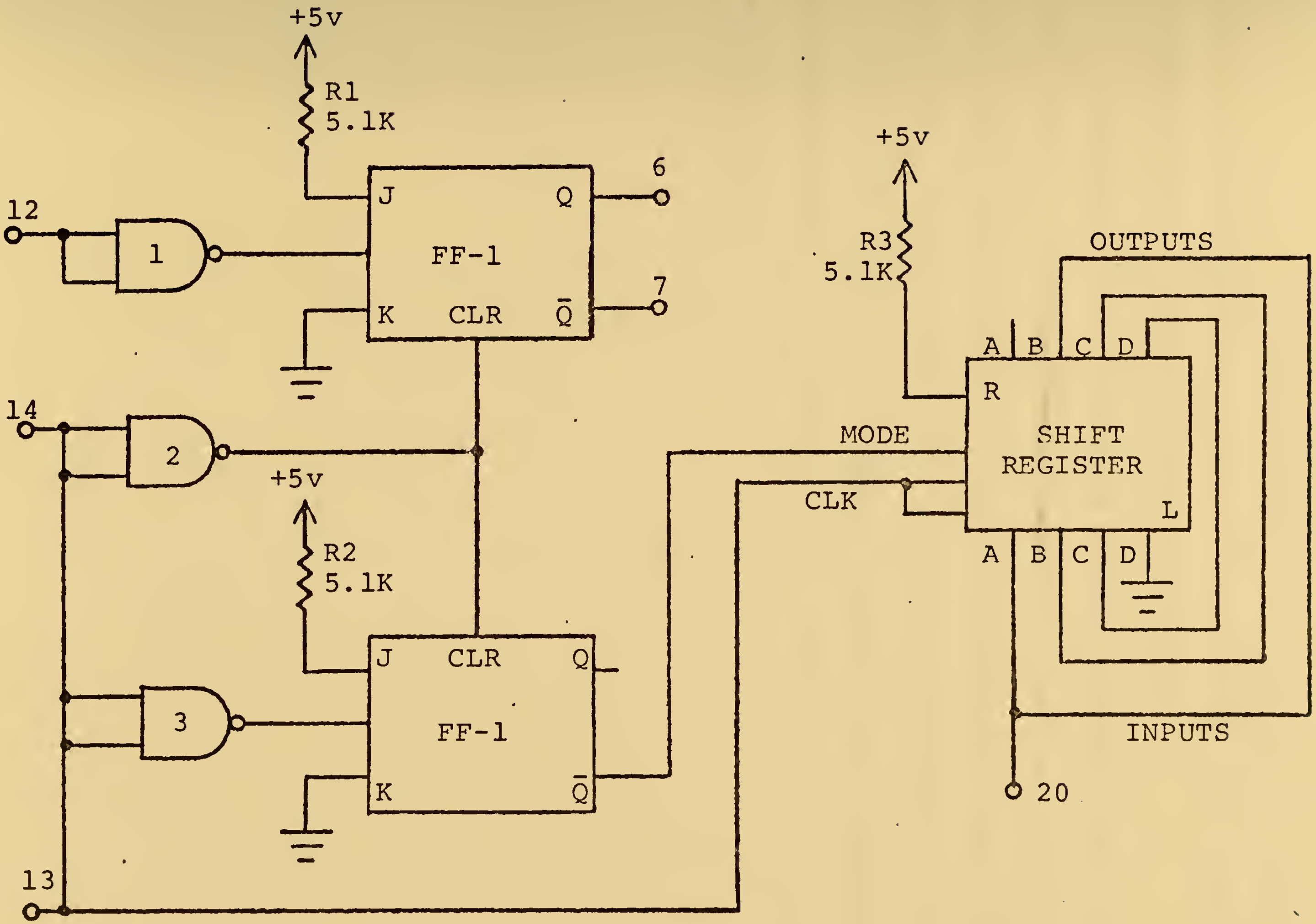


Figure 38. Feather Logic Block Diagram.

outputs of Z3 are logical zero. With pin 14 at a logical zero, two logical one pulses at pin 13 causes the A input of Z3 (pin 20) to become a logical one again. A logical zero at pin 20 indicates that the main lobe of a radar is illuminating the bistatic radar receiver.

A synchronized logical one pulse at pins 13 and 14 also clears FF-1. A pulse at pin 12 from the video unblanking circuit of module B11 is inverted through NAND gate one and clock FF-1, which causes the Q output to become a logical one and the $\bar{Q}$ output to become a logical zero. The Q output is fed through pin six to the video summing amplifier as the feather signal.

APPENDIX N

HEIGHT-TO-WIDTH CONVERTER (MODULE B11)

The height-to-width converter module was built by NAFI for use in their bistatic radar processor as a video unblanking and a threshold detection device. The following discussion was extracted for the most part from Ref. 1.

Side A of the module is a sample-and-hold circuit, Fig. 39. Any sample-and-hold circuit consists of three distinct subcircuits: (1) a switch, (2) a sample-and-hold section, (3) and an output circuit. The circuit described here uses a transistor driving an FET to form the switching section, while a capacitor performs the function of holding or storing the signal level. The output driver, Z1 in this case, is an HA-2600 operational amplifier which presents the stored value to a load with little distortion or delay.

Since it is desired that the normal condition of the switch be in the open or off condition, it is necessary to hold the gate of the FET at or above ground. This stipulation requires that Q1 be in the on condition in its normal state. Transistor Q1 is biased so that it remains on with as much as one volt on the base but is turned off with the base at four volts.

A positive triggering pulse of one microsecond duration from one shot Z2 of module B2 is used to turn Q1 off and, consequently, a negative 15 volts is applied to the gate of

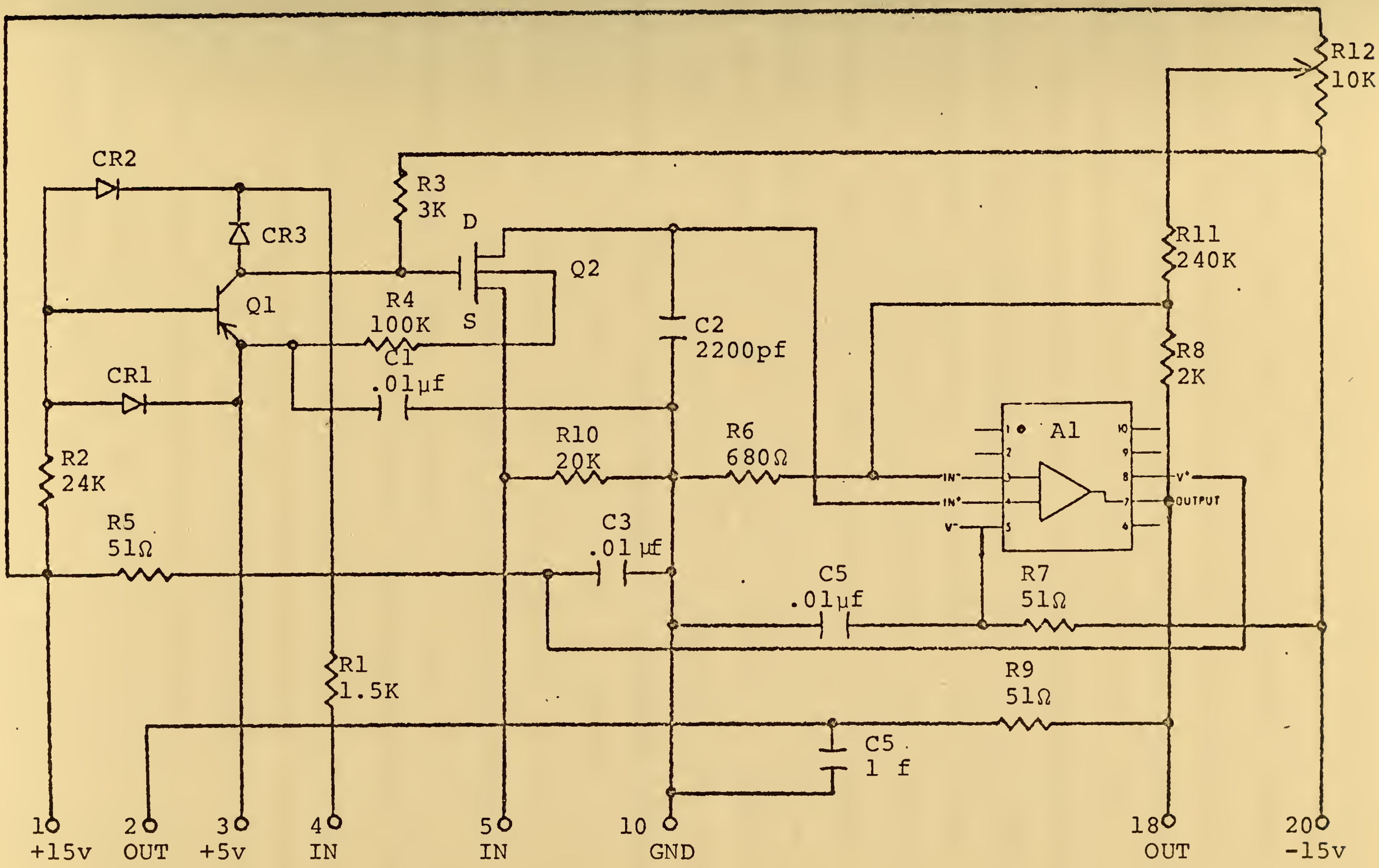


Figure 39. Height-to-width Converter Module - Side A.

Q2 turning it on. With Q2 on, a very small resistance is formed from the drain to source, and the stretched video pulse from module B10, which has been constantly present at the source, will now appear at the drain. The storage capacitor C2 charges to the level of the drain voltage, and within one microsecond, reaches 2/3 of its final value.

Transistor Q2 turns off after the one microsecond trigger pulse has passed and a veritable open circuit then exists between the drain and source. No discharge path is now present for C2 and its charge is held due to the high input impedance of the op amp. The op amp serves as a voltage follower and presents this stored level to the output where it is utilized by the video unblanking circuit on side B.

Diode CR1 serves to protect Q1 from reverse bias, while diodes CR2 and CR3 aid the transistor in switching speed by holding it out of saturation. Resistors R5 and R7 and capacitors C1, C3 and C4 serve to decouple the ±15 and +5 volt supplies. R1 is the input resistor for Q1 while R2 and R3 provide its bias. R4 protects Q2 from spurious high-voltage signals. C2 is the holding capacitor for the sample and hold and R10 provides a discharge path for C2 when Q2 is on. R9 and C5 serve as a low-pass filter for the output at pin 2. The combination of R11 and R12 is used to zero adjust the inherent offset voltage of the op amp Z1. R8, the feedback resistor of the op amp, and the input resistor R6 yield a gain of four.

Side B of the module performs two distinct functions, each of which utilizes a Fairchild 710 integrated differential comparator as shown in the schematic diagram of Fig. 40. Comparator Z2 performs the threshold-detection function, while Z3, in conjunction with the sample and hold circuit on Side A, performs the video unblanking function.

As a threshold detector, Z2 receives the stretched video pulse from module B10 on pin 3 where it is compared with a DC level on pin 2. This DC level is manually determined by trimpot R19 which allows a range from zero to about 0.64 volts to be fed to pin 2. Any pulse whose amplitude goes above the DC level generates a logical one pulse on pin 6 of the comparator. This output is applied to pin 14 of the feather logic module. When the video pulse amplitude decreases to below the manually determined DC level, the comparator output returns to logical zero.

Transistor Q3A serves to furnish the output logic of the comparator with enough drive to actuate other circuitry. Resistor R20 is added to enable the comparator output, which is an emitter follower stage, to return to logical zero quickly by sinking the necessary current. Resistor R22 is a compromise value between power dissipation and pulse rise time. Resistor R13 is incorporated to equalize the bias currents of the comparator inputs.

The second comparator, Z3, works in conjunction with the sample-and-hold circuit on side A. The output of the sample and hold, a DC level varying from zero to +4 volts,

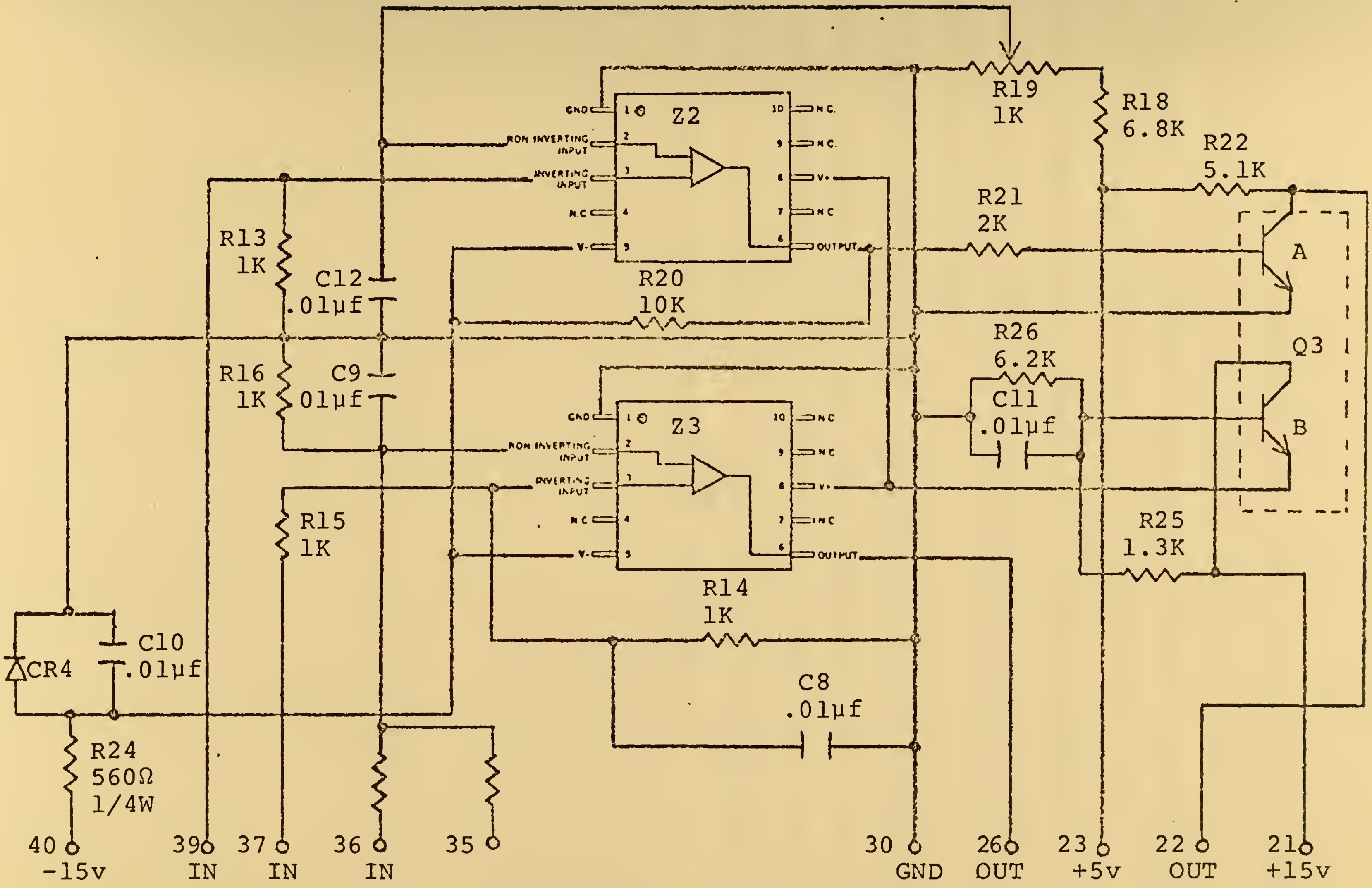


Figure 40. Height-to-width Converter Module - Side B.

is fed to pin 37 on the module through the voltage divider network of R14 and R15 which reduces the DC input to 1/2 its level (two volts maximum). The other input of Z3 (pin 2) is fed by a ramp voltage of from zero to 10 volts at module pin 36. The divider action of R16 and R23 reduces this to a maximum of two volts. The output of Z3 is a logical one whenever the output of the sample-and-hold circuit exceeds the magnitude of the ramp voltage, and is logical zero otherwise.

Transistor Q3B furnishes a supply voltage of +12 volts to both comparators, the base being biased at +12.5 volts by R25 and R26. Zener diode CR4 furnishes the -6.2 volts required by both comparators. Capacitors found throughout the circuitry provide the necessary decoupling.

APPENDIX O

AZIMUTH RAMP AND DC-VOLTAGE GENERATOR (MODULE B12)

This module was designed by the author. A ramp generator is triggered when a radar main lobe is received by the bistatic radar receiver and is retriggered each time the radar antenna looks at the receiver. The amplitude of the ramp is therefore proportional to the radar antenna sweep period. A sample-and-hold circuit samples the ramp voltage just before it is retriggered.

Side A consists of an integrator, a sample-and-hold circuit and two FET switches. One of the switches is used to start and stop the integrator while the other is used to control the sampling of the sample-and-hold circuit. Side B contains three one shots and two two-input NAND gates which are utilized as logic circuits to control the timing of the two FET switches on side A.

Side A, Fig. 41, contains two HA-2600 op amps. The first op amp, Z1, is configured as an integrator with R1 and R2 as a voltage divider which reduces -15 volts DC to -3.75 volts. This voltage is tied to the inverting input of Z1 through the input resistor R3. C3 serves as the integrating capacitor for Z1. One of the FET switches on the Siliconix DG133L, which is a 2-channel driver with SPST FET switches, in series with R4 is shunted across C3 as a means of starting and stopping integration. R4 provides the discharge path

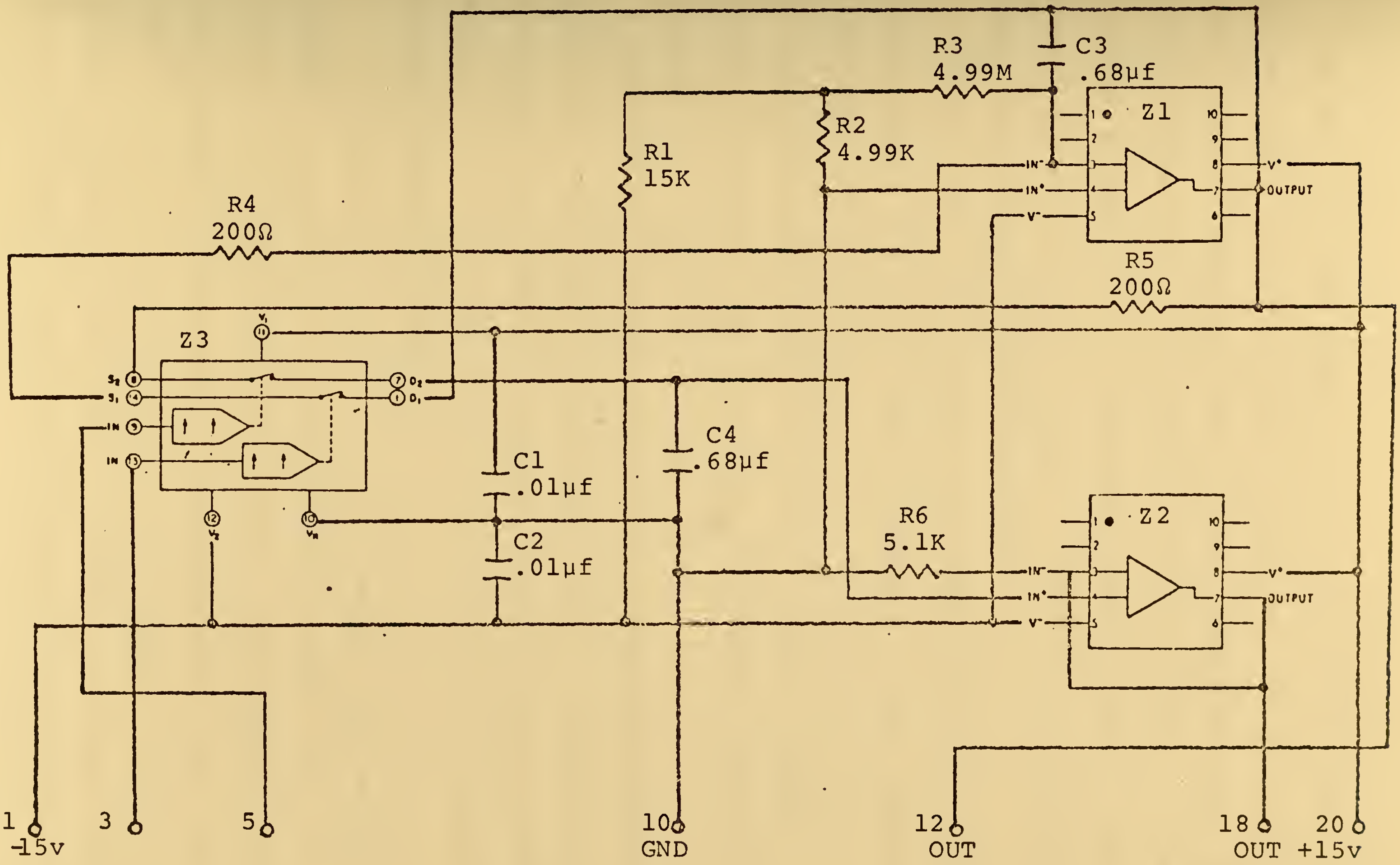


Figure 41. Azimuth Ramp and DC Voltage Generator Module - Side A.

for C3 when the FET switch is on. The other FET switch is in the path from the output of Z1 to the non-inverting input of the sample-and-hold output op amp, Z2. C4 is shunted from the non-inverting input of Z2 to ground and acts as the holding capacitor in the sample-and-hold circuit. R5 serves the same purpose for C4 as R4 does for C3. R6 ties the inverting input of Z2 to ground. C1 and C2 are decoupling capacitors for the ±15 volt supplies.

Side B, Fig. 42, contains four Texas Instruments integrated circuits. Z4 is an SN5400 quadruple 2-input positive NAND gate, while Z5, Z6 and Z7 are SN54121 one shots. C5 is the decoupling capacitor for the +5 volt DC supply. R7 and C6, R8 and C7, and R9 and C8 are external timing components for Z5, Z6 and Z7 respectively.

Figure 43 is a block diagram depicting both sides of the module and their interconnections, and Fig. 44 shows the waveforms to be found at strategic locations on the module. Reference to these two figures will facilitate understanding of the following discussion.

A logical zero pulse, from the feather logic module, is applied to pin 24 of the module when the main lobe of a radar signal is received, Fig. 44(a). The duration of this pulse depends on the length of time the main lobe of the radar illuminates the bistatic radar receiver. NAND gate G1 inverts the pulse, Fig. 44(b). The positive going edge of the pulse from G1 triggers one shot Z5 which produces a 0.3 second logical zero pulse at the $\bar{Q}$ output, Fig. 44(c). The

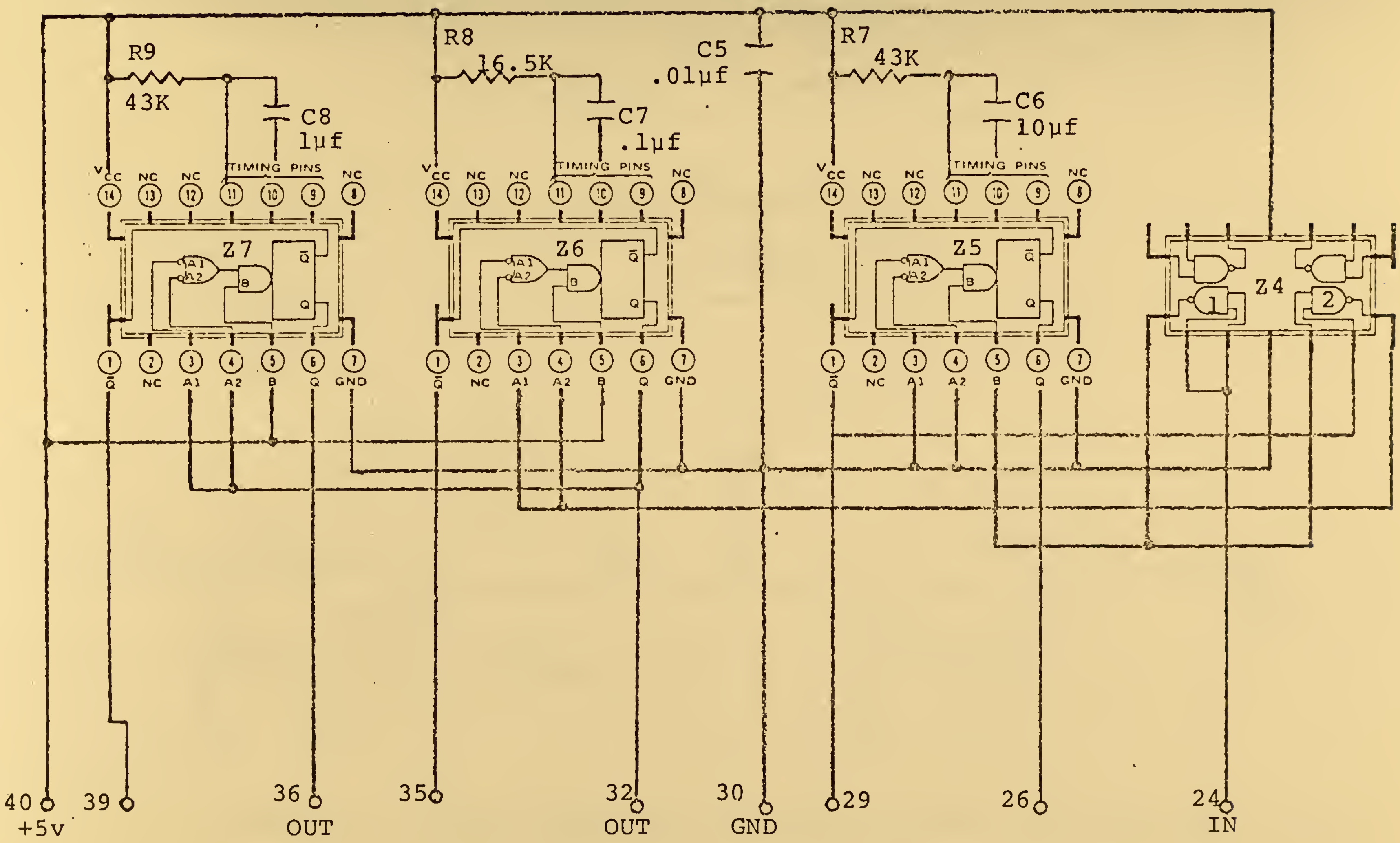


Figure 42. Azimuth Ramp and DC Voltage Generator Module - Side B.

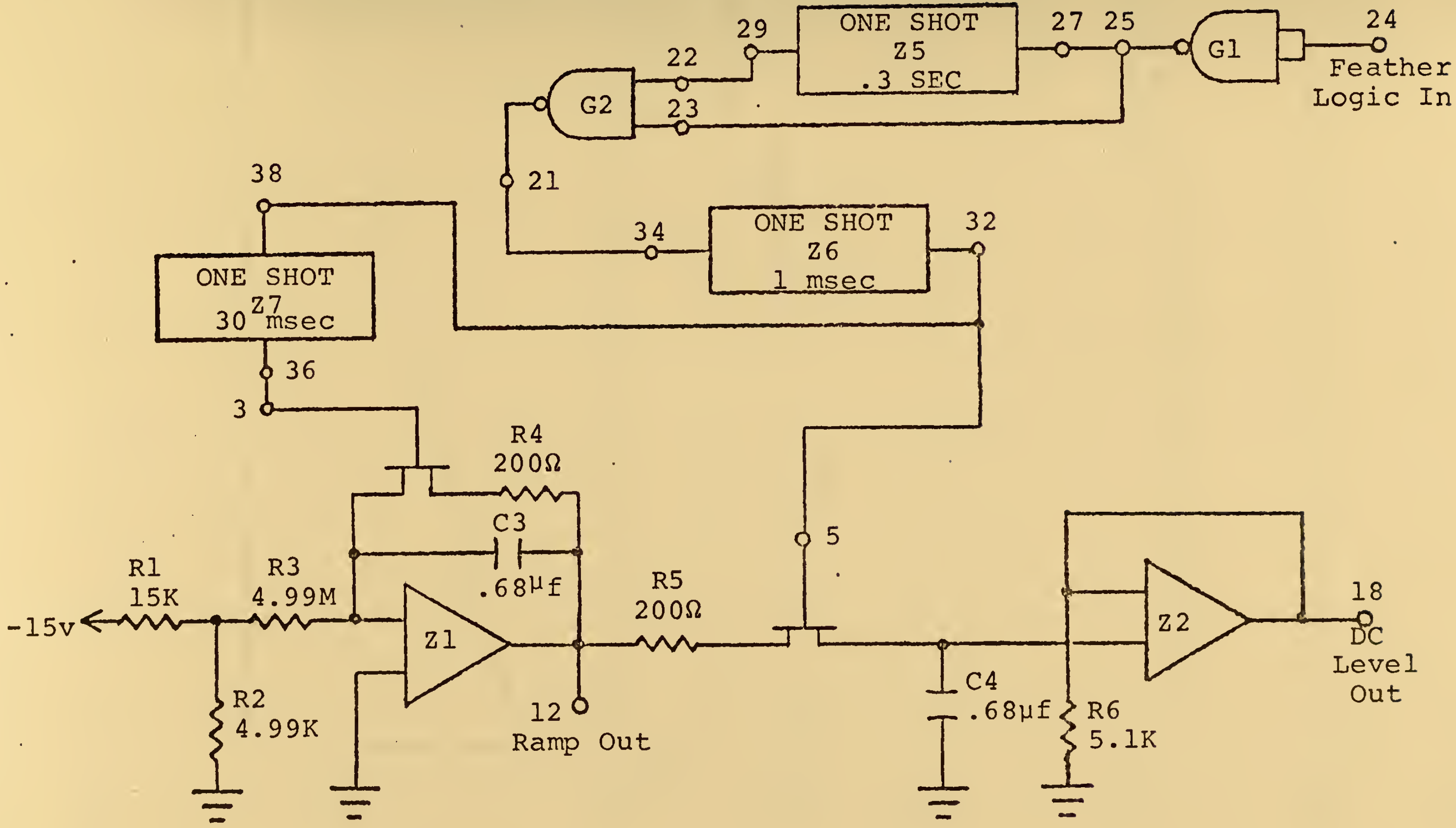


Figure 43. Azimuth Ramp and DC Voltage Generator Block Diagram.

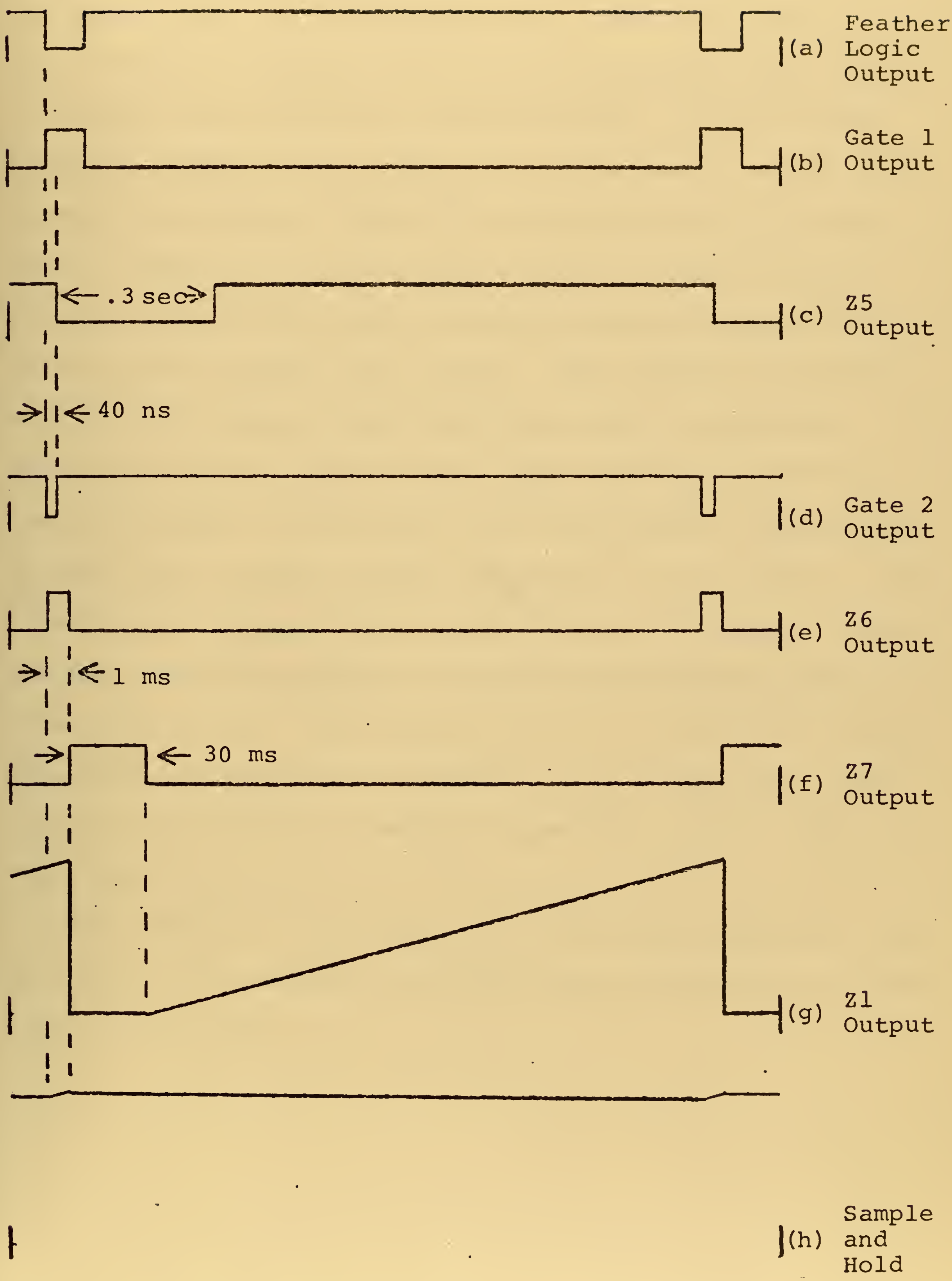


Figure 44. Azimuth Ramp and DC Voltage Generator Waveforms.

output of Z5 is applied to one of the inputs to NAND gate G2. The other input to G2 comes from G1. The output of G2, Fig. 44(d), is a logical one at all times except when both its inputs are logical one simultaneously. As can be seen from Fig. 44(b) and (c) this only occurs during the 40 nanosecond time period it takes Z5 to switch after it is triggered. The negative going edge of the G2 output triggers one shot Z6 which produces a one millisecond logical one pulse at the Q output, Fig. 44(e). The positive going edge of this pulse turns on the FET switch which enables the sampling capacitor (C4) of the sample and hold circuit for one millisecond. During this time the capacitor charges up to the output voltage of the integrator Z1, Fig. 44(h). The negative going edge of the one millisecond Z6 output triggers one shot Z7 which produces a 30 millisecond logical one pulse, Fig. 44(f). This pulse turns on the FET switch which allows the integrating capacitor of Z1 to discharge. After the 30 milliseconds, Z1 begins to generate another ramp, Fig. 44(g).

The reason for the relatively long pulse duration of the Z5 output is to prevent the circuit from retriggering on side lobes of the radar.

APPENDIX P

MOTOR CONTROL ERROR AMPLIFIER (MODULE B13)

This module was designed by the author. Its function is to control the speed of the azimuth drive motor for the PPI display in order to synchronize it with the rotation of the antenna of the radar. A control voltage to give approximately the correct speed is set in manually with the SPR set potentiometer on the front panel. An error correction circuit detects any difference between PPI azimuth sweep speed and radar antenna speed, and develops a positive or negative error voltage which is added to the voltage from the potentiometer in the correct polarity to reduce the motor speed error. A more detailed description of the operation of the circuit follows.

Side B of the module is blank. Side A, Fig. 45, contains two HA-2600 op amps. Z1 is configured as a differential integrator and Z2 as an integrating amplifier. C1 and C2 are decoupling capcitors for the ±15 volt DC supplies. R1 and C3 and R2 and C4 are low-pass filters on the non-inverting and inverting inputs to Z1. CR1 and C5 are parallel feedback elements for Z1. CR2 controls the direction of current flow between Z1 and Z2. R4, R5 and R6 controls the direction of current flow between Z1 and Z2. R4, R5 and R6 are input resistors for the inverting input to Z2. While C6 and R7 are its parallel feedback elements.

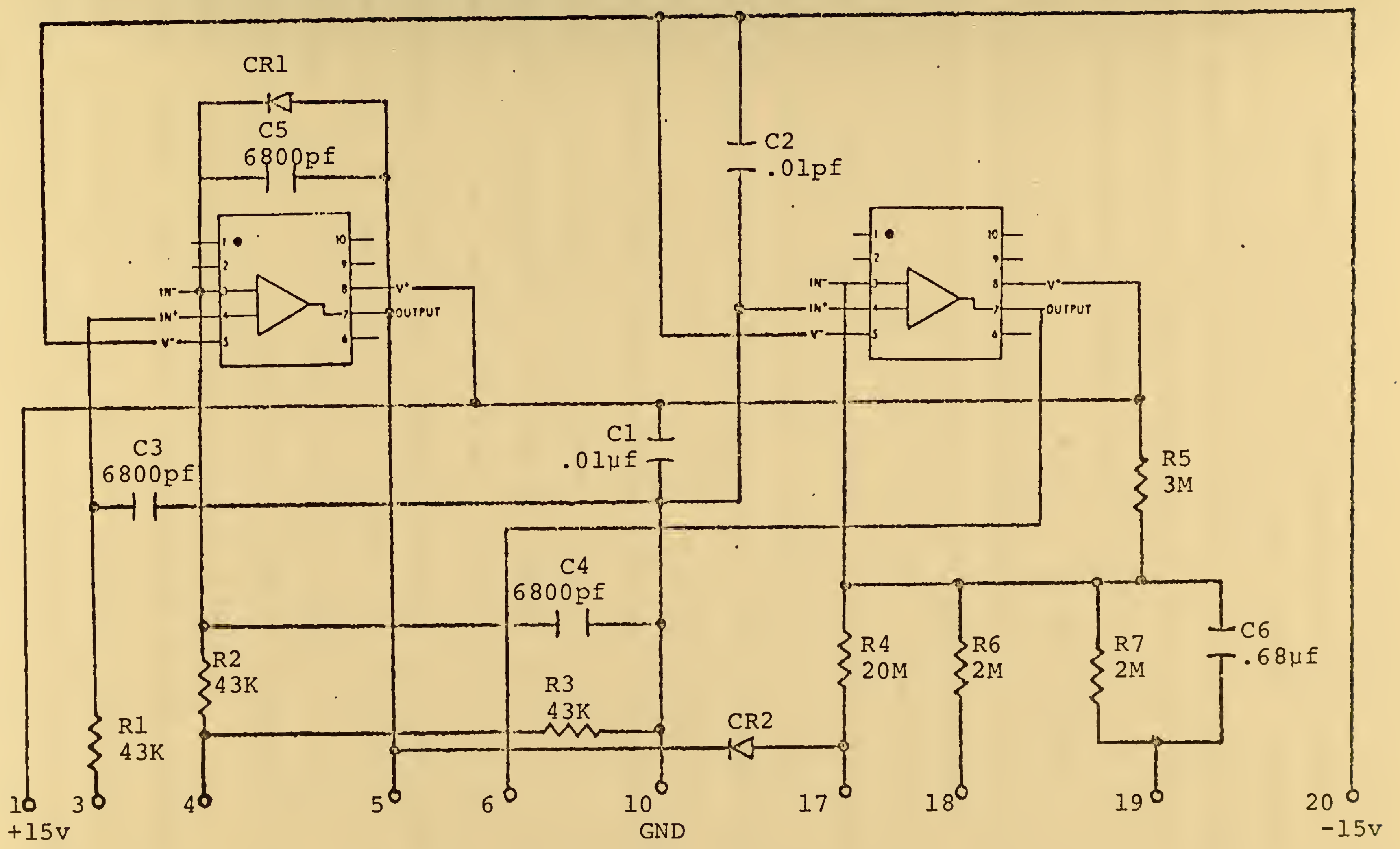


Figure 45. Motor Control Error Amplifier Module - Side A.

Figure 46 shows the motor control circuit in its entirety, including components which are external to this module, to facilitate explanation of how the module works. The additional components are a +24 volt supply, the DC motor itself, power transistor Q1, diodes CR3 and CR4, which protect Q1 from negative current surges from the motor, and R8, which is a current limiter for the collector circuit of Q1.

The sample-and-hold output of module B12 is fed to the linear portion of the sine/cosine potentiometer which is turned by the motor. The output from the linear potentiometer is a linear ramp voltage which is identical in magnitude to the azimuth ramp output of module B12. However, the slope of the linear potentiometer ramp, which is dependent upon the speed with which the motor is turning the sine/cosine potentiometer, is not necessarily the same as that of the azimuth ramp; and the phase difference, which is dependent upon whether or not the two ramps start at the same time, is not necessarily zero. The purpose of the motor-control circuit is to correct both of these discrepancies so that the two ramps are identical in magnitude, slope and phase. This would insure that the sweep of the PPI display was exactly synchronized in speed and phase with the antenna rotation of the radar being received.

The linear ramp from the potentiometer is applied to pin three of the module and the azimuth ramp from module B12 is applied to pin 4. Voltage differences between these inputs are integrated and appear at the output of Z1 as error

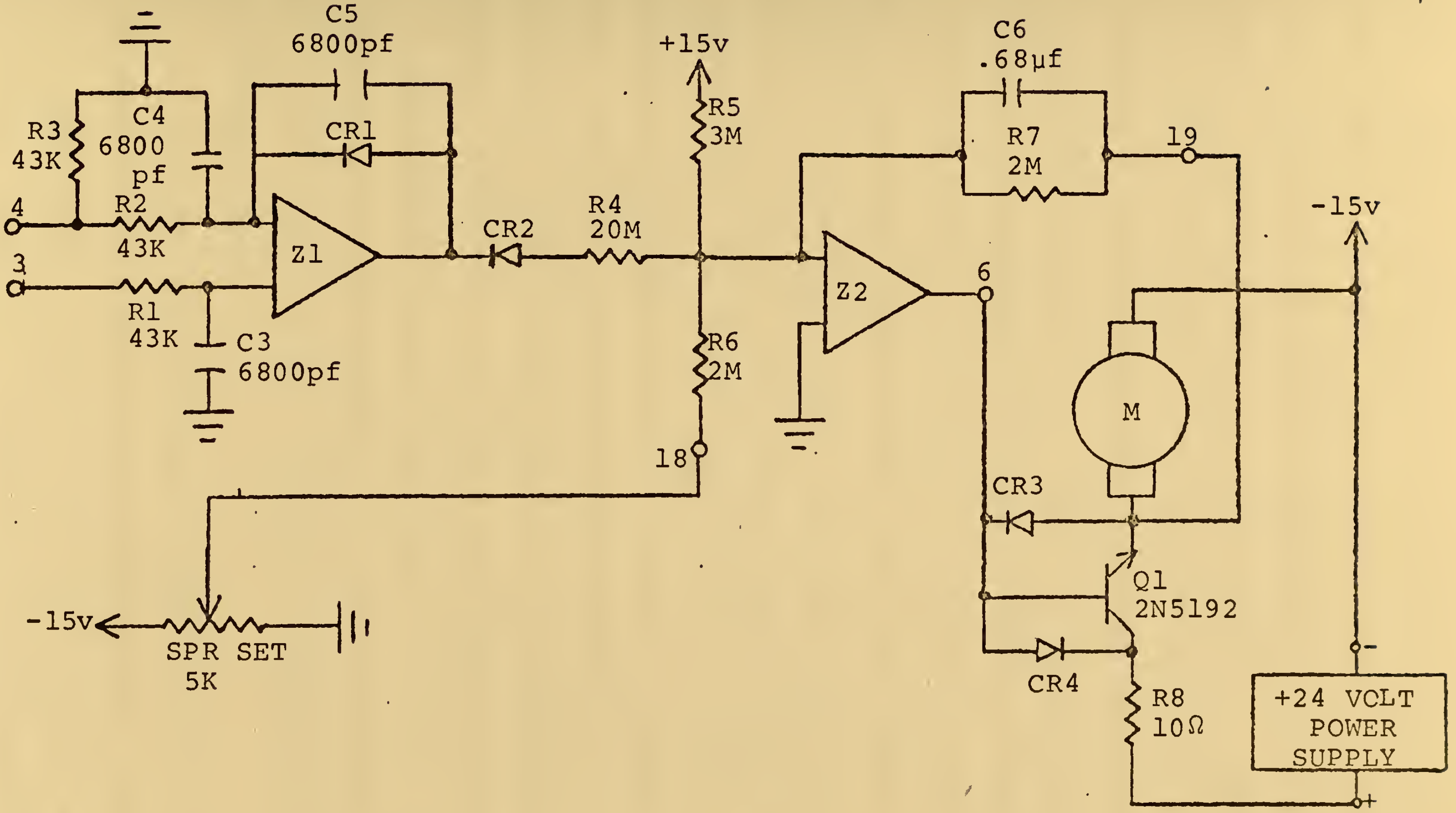


Figure 46. Motor Control Circuit.

voltages. However, the gain of the differential integrator Z1 is such that the output very rapidly goes into either negative or positive saturation depending on whether the non-inverting or inverting input is more positive. Diode CR1 acts to prevent Z1's output from reaching positive saturation, because as soon as the output voltage exceeds the inverting inputs voltage by 0.7 volts the diode conducts, and Z1 becomes an extremely low-gain amplifier. CR2 conducts only when Z1's output is at least 0.7 volts less than the voltage on the other side of CR2. The total effect of the two diodes is to reduce hunting (the motor alternately speeding up and slowing down without ever settling down). This tends to make the SPR set potentiometer setting rather critical since the error voltage to speed up the motor has much more effect than the one to slow it down.

Z2 sums the three scaled inputs to its inverting input and amplifies them, with C6 having the effect of slowing down the response of the amplifier since the motor cannot make instantaneous speed changes. The more positive the voltage at the output of Z2, the more Q1 conducts and the faster the motor goes.

This circuit was the last one designed for the system and time limitations precluded its optimization. Further work to prevent hunting without use of CR1 and CR2 and to reduce the time required to achieve synchronization would improve the system.

APPENDIX Q

SYSTEM WIRING CONNECTIONS

The operating controls on the front panel, the inputs and outputs on the rear panel, the motor circuit, the sine/cosine potentiometer and the modules are interconnected to form the bistatic radar system. These interconnections are discussed below.

A. FRONT PANEL CONNECTIONS

The internal view of the front panel is shown in Fig. 47. The wiring connections to the controls are listed in Table V.

B. REAR PANEL CONNECTIONS

The rear panel has wiring connections on both the inside and the outside. These connections are discussed in the following paragraphs.

1. Internal Rear Panel Connections

The internal view of the rear panel is shown in Fig. 48. The internal wiring connections are listed in Table VI.

2. External Rear Panel Connections

The external view of the rear panel is shown in Fig. 12 and the wiring connections are discussed in section IV.B with the exception of the connections from the 36-pin input/output connector. These connections are listed in Table VII.

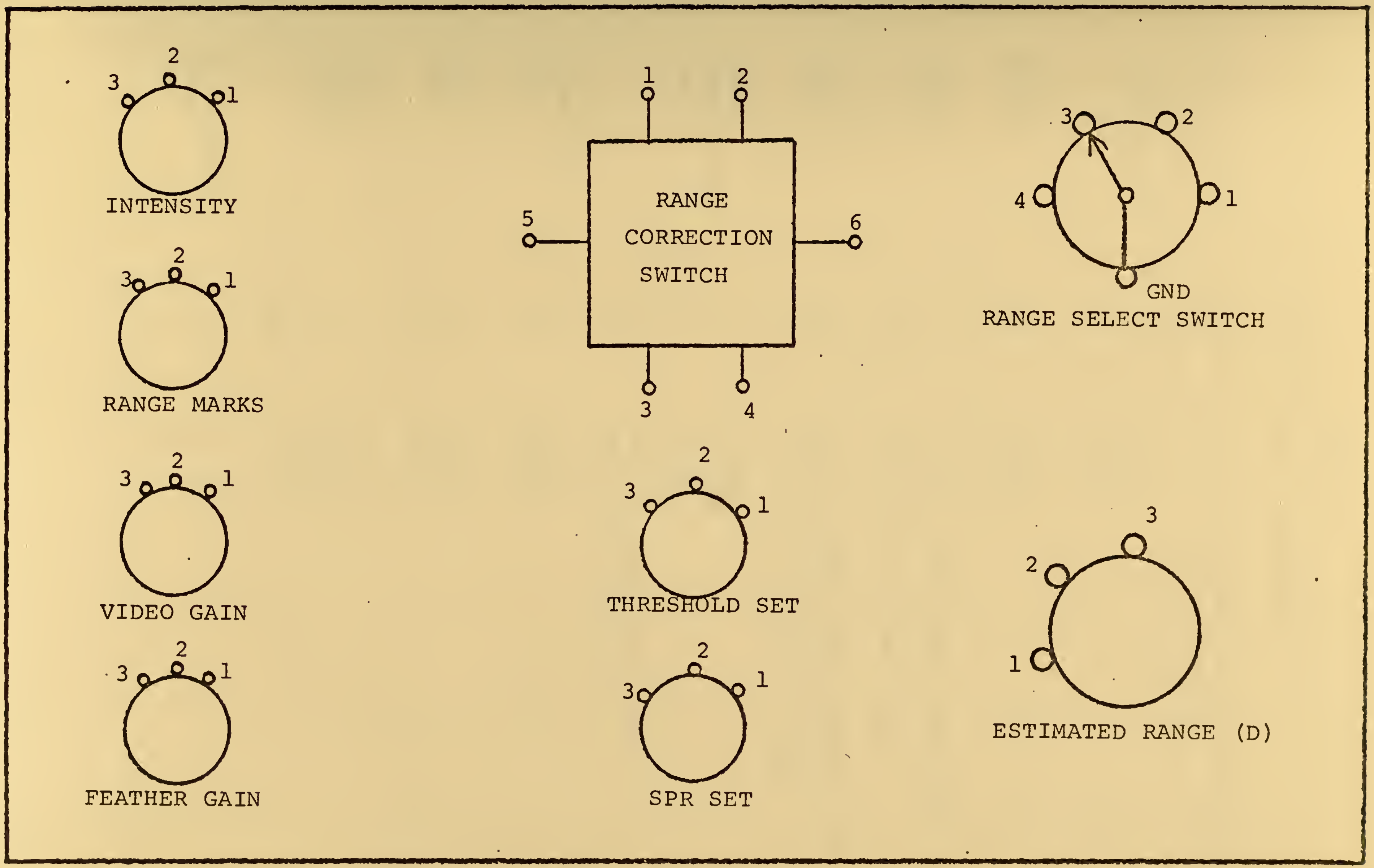


Figure 46. Front Panel Layout.

TABLE V

FRONT PANEL CONNECTIONS

Control	Pin	Connected To
Intensity	1	A2-35
	2	A2-34
	3	A2-33
Range Marks	1	A2-40
	2	A2-37
	3	A2-36
Video Gain	1	A1-38, Rear panel video GND
	2	A1-37
	3	Rear panel video input
Feather Gain	1	A2-39, Rear panel feather GND
	2	Test signal switch pin 2
	3	Rear panel feather input
Range Correction Switch	1	A1-26
	2	A1-27
	3	A1-28
	4	A1-29
	5	A2-21, Rear panel pin b
	6	Rear panel pin M
Threshold Set	1	A2-25
	2	A1-12
	3	A2-24
SPR Set	1	A2-13
	2	A2-15
	3	A2-14
Range Select Switch	1	A1-22
	2	A1-23
	3	A1-24
	4	A1-25
	GND	A1-39
Estimated Range (D)	1	A2-22
	2	A2-23
	3	NC

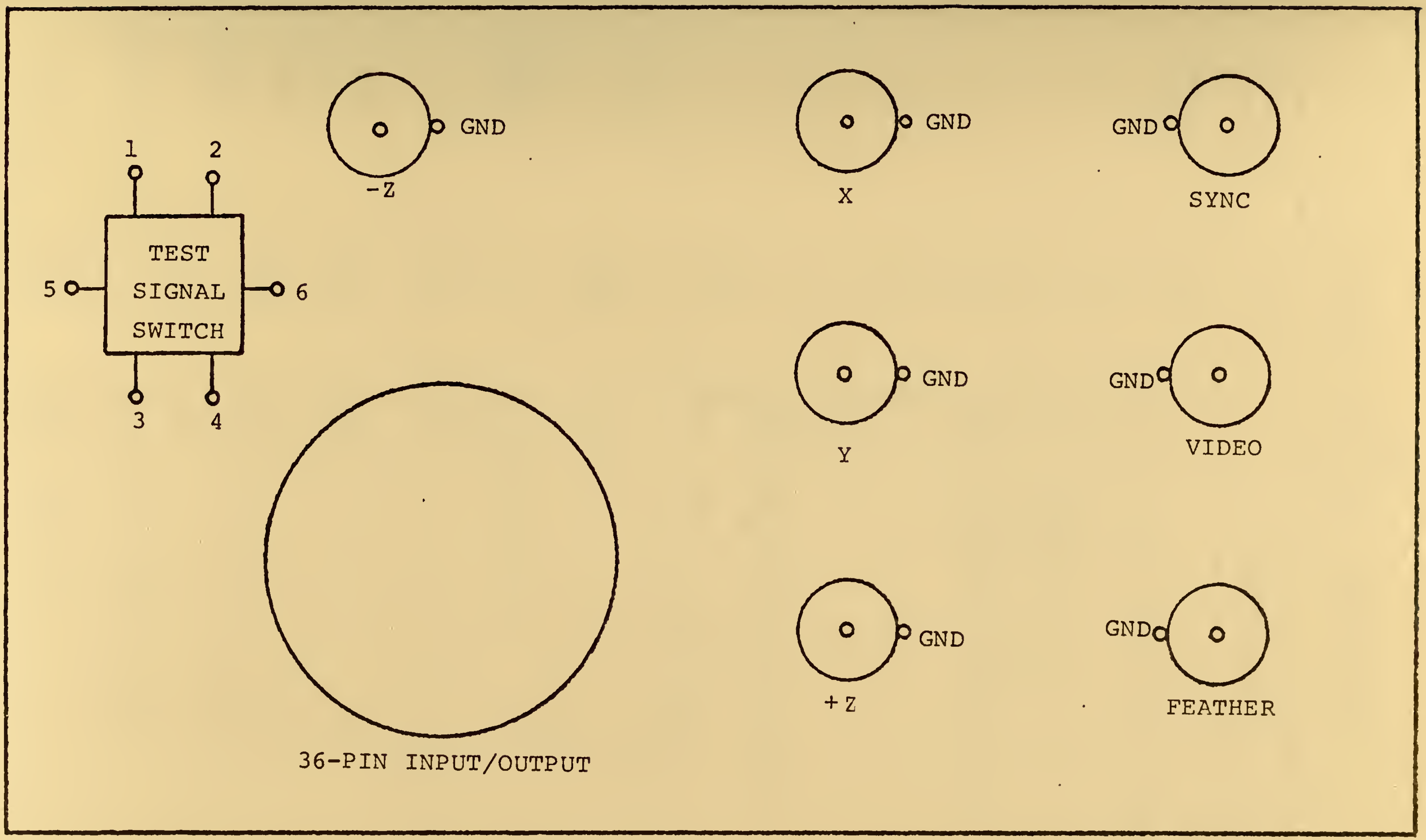


Figure 48. Internal Rear Panel Layout.

TABLE VI

INTERNAL REAR PANEL CONNECTIONS

Control/ Connector	Pin	Connected To
36-Pin Connector	A-D	NC
	E	A2-19
	F	Motor driver's collector resistor
	G	A1-30
	H	A1-20, A1-40
	J	A1-3, through A1-10
	K	A1-1, A1-21
	L	A1-13 through A1-18
	M	Range correction switch pin 6
	N	Chassis GND
	P	NC
	R-W	NC
	X	A2-20
	Y	A2-18
	Z	A1-31
	a	A1-32
	b	Range correction switch pin 5
	c	A2-26
	d-g	NC
	h	Motor driver's emitter
	j	NC
-Z Out	-Z	A2-30
	GND	A2-29
Test Signal Switch	1	Sync In
	2	Feather gain in
	3	A2-27
	4	A2-28
	5	A1-2
	6	A2-38
X Out	X	A1-33
	GND	A1-35
Y Out	Y	A1-34
	GND	A1-36
Z Out	Z	A2-32
	GND	A2-31
Sync In	Sync	Test signal switch pin 1
	GND	A1-19
Video In	Video	Video gain pin 3
	GND	Video gain pin 1
Feather In	Feather	Feather gain pin 3
	GND	Feather gain pin 1

TABLE VII

EXTERNAL REAR PANEL CONNECTIONS FOR 36-PIN CONNECTOR

Pin	Wire Color	Connected To
A-D		NC
E	Green	Sin/cos linear pot (CCW)
F	Orange	+24 VDC supply
G		NC
H	Purple	-15 VDC supply
J	Black	GND
K	Wh/Red/Gr	+15 VDC supply
L	Red	+5 VDC supply
M	Wh/Blk/Blu	Sin/cos pot ($-E_{in}$)
N	Black	Chassis GND
P		NC
R-W		NC
X	Blue	Sin/cos linear pot (CW)
Y	Brown	Sin/cos linear pot (Wiper)
Z	Wh/Brn/Grn	Sin/cos pot (sin ϕ out)
a	Wh/Blu	Sin/cos pot (cos ϕ out)
b	Wh/Or	Sin/cos pot ($+E_{in}$)
c	Wh/Blk/Pur	Sin/cos pot (GND)
d-g		NC
h	Wh/Blk/Blu	Motor GND
j		NC

C. MODULE CONNECTIONS

The modules are connected to the rest of the system through the input power connector and the input connector which are discussed in appendices A and B. Interconnections between the modules are accomplished by connecting wires between the pins protruding from the wirewrap plate. These interconnections are called the "wirewrap" and may be made either by hand, using a special tool, or by a computer controlled machine. The wirewrap connections for the modules in the processor are listed in Tables VIIIa through VIIIp.

TABLE VIIIa

WIREWRAP PIN CONNECTIONS FOR MODULE A1

Pin No.	Connected To	Pin No.	Connected To
1	B3-1	21	NC
2	B1-21	22	B2-32
3	B1-30	23	B2-33
4	B3-10	24	B2-35
5	B5-10	25	B2-31
6	B1-10	26	B5-12
7	A2-13	27	B5-2,B5-18
8	B6-10	28	B8-8
9	B10-10,B12-10	29	B6-18
10	A2-19,B10-30	30	NC
11	B3-11	31	B5-26
12	B1-22	32	B5-37
13	A2-24	33	B5-23
14	B1-40	34	B5-36
15	B10-15	35	B5-30
16	A3-4	36	B5-31
17	NC	37	B7-24
18	NC	38	B7-30
19	B1-30	39	B2-30
20	B3-20	40	NC

TABLE VIIIb

WIREWRAP PIN CONNECTIONS FOR MODULE A2

Pin No.	Connected To	Pin No.	Connected To
1	NC	21	B3-4
2	NC	22	B8-6
3	NC	23	B8-16
4	NC	24	A1-13
5	NC	25	A1-19
6	NC	26	B5-10
7	NC	27	A3-13
8	NC	28	A3-15
9	NC	29	B7-30
10	NC	30	B7-36
11	NC	31	B7-30
12	NC	32	B7-33
13	A1-7	33	A1-21
14	A1-20	34	B7-23
15	B13-18	35	A1-40
16	B13-19	36	B3-37
17	B13-6	37	B7-25
18	B13-4	38	B10-34
19	A1-10,B12-10, B13-10	39	B10-30
		40	B3-10,B7-10
20	B12-18		

TABLE VIIIc

WIREWRAP PIN CONNECTIONS FOR MODULE A3

Pin No.	Connected To	Pin No.	Connected To
1	NC	21	NC
2	NC	22	NC
3	NC	23	NC
4	A1-16	24	NC
5	NC	25	NC
6	NC	26	NC
7	NC	27	NC
8	NC	28	NC
9	NC	29	NC
10	A1-19,A2-39	30	NC
11	NC	31	NC
12	NC	32	NC
13	A2-27	33	NC
14	NC	34	NC
15	A2-28	35	NC
16	NC	36	NC
17	NC	37	NC
18	NC	38	NC
19	NC	39	NC
20	NC	40	NC

TABLF VIIId

WIREWRAP PIN CONNECTIONS FOR MODULE A4

Pin No.	Connected To	Pin No.	Connected To
1	B1-21	21	B7-24
2	B1-27	22	B7-25
3	B2-3	23	B7-26
4	B3-15	24	B7-27
5	B3-4	25	B7-33
6	B4-9	26	B7-36
7	B5-18	27	B10-34
8	B5-5	28	B10-37
9	NC	29	B2-19
10	B8-18	30	B11-18
11	NC	31	B11-22
12	B8-19	32	B11-26
13	B8-6	33	B10-20
14	B8-8	34	NC
15	B6-18	35	NC
16	B5-26	36	NC
17	B5-23	37	NC
18	B5-37	38	NC
19	B5-36	39	NC
20	B7-23	40	NC

TABLE VIIIe

WIREWRAP PIN CONNECTIONS FOR MODULE B1

Pin No.	Connected To	Pin No.	Connected To
1	NC	21	A1-2
2	NC	22	A1-12
3	NC	23	NC
4	NC	24	NC
5	NC	25	NC
6	NC	26	B1-27
7	NC	27	B2-5
8	NC	28	B1-21
9	NC	29	NC
10	NC	30	A1-3
11	NC	31	NC
12	NC	32	NC
13	NC	33	NC
14	NC	34	NC
15	NC	35	NC
16	NC	36	NC
17	NC	37	NC
18	NC	38	NC
19	NC	39	NC
20	NC	40	A1-14

TABLE VIIIf

WIREWRAP PIN CONNECTIONS FOR MODULE B2

Pin No.	Connected To	Pin No.	Connected To
1	B1-40	21	B2-1
2	NC	22	NC
3	B3-8	23	B4-17
4	B2-10,B2-17	24	NC
5	B1-26	25	NC
6	B2-18	26	NC
7	NC	27	NC
8	NC	28	B4-14
9	NC	29	NC
10	B1-30	30	B2-10
11	NC	31	A1-25
12	NC	32	A1-22
13	NC	33	A1-23
14	NC	34	NC
15	NC	35	A1-24
16	NC	36	B4-4
17	B2-4	37	NC
18	B2-6	38	NC
19	B10-13,B11-14	39	B4-13
20	NC	40	NC

TABLE VIIIg

WIREWRAP PIN CONNECTIONS FOR MODULE B3

Pin No.	Connected To	Pin No.	Connected To
1	A1-1	21	B3-1
2	B2-1	22	B3-19
3	B3-38	23	B3-18
4	A2-21	24	B3-17
5	B3-36	25	B3-16
6	B3-35	26	NC
7	NC	27	NC
8	B2-3	28	NC
9	B2-32	29	NC
10	A1-4	30	B3-10
11	A1-11	31	NC
12	NC	32	B3-9
13	NC	33	NC
14	B7-27	34	NC
15	B4-28,B5-6	35	B3-6
16	B3-25	36	B3-5
17	B3-24	37	A2-36
18	B3-23	38	B3-3
19	B3-22	39	B3-2
20	A1-20	40	B3-20

TABLE VIIIh

WIREWRAP PIN CONNECTIONS FOR MODULE B4

Pin No.	Connected To	Pin No.	Connected To
1	B3-1	21	B4-1
2	NC	22	NC
3	B4-36	23	NC
4	B2-36	24	NC
5	NC	25	NC
6	NC	26	NC
7	NC	27	NC
8	B4-37	28	B3-15
9	B5-12,B8-17,A1-26	29	NC
10	B5-10,B6-30	30	NC
11	B3-11	31	NC
12	B3-2	32	NC
13	B2-39	33	NC
14	B2-28	34	NC
15	B4-19	35	NC
16	NC	36	B4-3
17	B2-23	37	B4-8
18	NC	38	NC
19	B6-36	39	NC
20	B3-20	40	B4-20

TABLE VIIIi

WIREWRAP PIN CONNECTIONS FOR MODULE B5

Pin No.	Connected To	Pin No.	Connected To
1	B4-1	21	B5-20
2	B5-18	22	NC
3	NC	23	A1-33
4	NC	24	NC
5	B8-9	25	NC
6	B3-15	26	A1-31
7	NC	27	NC
8	NC	28	NC
9	NC	29	NC
10	A1-5	30	A1-35,B5-31
11	NC	31	B5-10,A1-36
12	A1-26,B4-9	32	NC
13	B6-21	33	NC
14	NC	34	NC
15	NC	35	NC
16	NC	36	A1-34
17	NC	37	A1-32
18	A1-27,B5-2,B8-3	38	NC
19	NC	39	NC
20	B4-20	40	B5-1

TABLE VIIIj

WIREWRAP PIN CONNECTIONS FOR MODULE B6

Pin No.	Connected To	Pin No.	Connected To
1	B5-1	21	B5-13
2	B5-36	22	B6-1
3	NC	23	B6-40
4	NC	24	NC
5	B8-18	25	NC
6	NC	26	NC
7	NC	27	NC
8	NC	28	NC
9	NC	29	NC
10	A1-8	30	B4-10
11	NC	31	NC
12	B8-8	32	NC
13	NC	33	NC
14	NC	34	NC
15	NC	35	NC
16	NC	36	B4-19
17	NC	37	NC
18	A1-29	38	NC
19	NC	39	NC
20	B6-40	40	B5-20

TABLE VIIIk

WIREWRAP PIN CONNECTIONS FOR MODULE B7

Pin No.	Connected To	Pin No.	Connected To
1	NC	21	NC
2	NC	22	A1-21
3	NC	23	A2-34
4	NC	24	A1-37
5	NC	25	A2-37
6	NC	26	B10-6
7	NC	27	B3-14
8	NC	28	NC
9	NC	29	NC
10	NC	30	A1-38,A2-29,A2-31, A2-39,A2-40
11	NC	31	NC
12	NC	32	NC
13	NC	33	A2-32
14	NC	34	NA
15	NC	35	NC
16	NC	36	A2-30
17	NC	37	NC
18	NC	38	NC
19	NC	39	NC
20	NC	40	A1-40

TABLE VIIIℓ

WIREWRAP PIN CONNECTIONS FOR MODULE B8

Pin No.	Connected To	Pin No.	Connected To
1	B7-22	21	NC
2	B8-19	22	NC
3	B5-18	23	NC
4	B8-19	24	NC
5	NC	25	NC
6	A2-22	26	NC
7	NC	27	NC
8	A1-28,B6-12	28	NC
9	B5-5	29	NC
10	B5-30	30	NC
11	NC	31	NC
12	NC	32	NC
13	NC	33	NC
14	B8-39	34	NC
15	B8-35	35	B8-15
16	A2-23	36	NC
17	B4-9	37	NC
18	B6-5	38	B8-1
19	B8-2,B8-4	39	B8-14
20	B7-40	40	B8-20

TABLE VIIIm

WIREWRAP PIN CONNECTIONS FOR MODULE B10

Pin No.	Connected To	Pin No.	Connected To
1	NC	21	B10-15
2	NC	22	NC
3	NC	23	NC
4	NC	24	NC
5	NC	25	NC
6	B7-26	26	NC
7	NC	27	NC
8	NC	28	NC
9	NC	29	NC
10	A1-9,B11-30	30	A1-10,A2-39,B11-10
11	NC	31	NC
12	B11-26	32	NC
13	B2-19	33	NC
14	B11-22	34	A2-38
15	A1-15	35	NC
16	NC	36	NC
17	NC	37	B11-5,B11-39
18	NC	38	NC
19	NC	39	NC
20	B12-24	40	NC

TABLE VIIIn

WIREWRAP PIN CONNECTIONS FOR MODULE B11

Pin No.	Connected To	Pin No.	Connected To
1	B8-1	21	B11-1
2	NC	22	B10-14
3	B10-21	23	B11-3
4	B2-19	24	NC
5	B10-37	25	NC
6	NC	26	B10-12
7	NC	27	NC
8	NC	28	NC
9	NC	29	NC
10	B10-30	30	B10-10
11	NC	31	NC
12	NC	32	NC
13	NC	33	NC
14	NC	34	NC
15	NC	35	NC
16	NC	36	B4-9
17	NC	37	B11-18
18	B11-37	38	NC
19	NC	39	B10-37
20	B8-40	40	B11-20

TABLE VIIIo

WIREWRAP PIN CONNECTIONS FOR MODULE B12

Pin No.	Connected To	Pin No.	Connected To
1	B11-40	21	NC
2	NC	22	NC
3	B12-36	23	NC
4	NC	24	B10-20
5	B12-32	25	NC
6	NC	26	NC
7	NC	27	NC
8	NC	28	NC
9	NC	29	NC
10	A2-19	30	A1-9
11	NC	31	NC
12	B13-3	32	B12-5
13	NC	33	NC
14	NC	34	NC
15	NC	35	NC
16	NC	36	B12-3
17	NC	37	NC
18	A2-20	38	NC
19	NC	39	NC
20	B11-21	40	B11-3

TABLE VIIIp

WIREWRAP PIN CONNECTIONS FOR MODULE B13

Pin No.	Connected To	Pin No.	Connected To
1	B12-20	21	NC
2	NC	22	NC
3	A2-18	23	NC
4	B12-12	24	NC
5	NC	25	NC
6	A2-17	26	NC
7	NC	27	NC
8	NC	28	NC
9	NC	29	NC
10	A2-19	30	NC
11	NC	31	NC
12	NC	32	NC
13	NC	33	NC
14	NC	34	NC
15	NC	35	NC
16	NC	36	NC
17	NC	37	NC
18	A2-15	38	NC
19	A2-16	39	NC
20	B12-1	40	NC

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2b. GROUP

REPORT TITLE

THE DESIGN AND FABRICATION OF A SIMPLIFIED BISTATIC RADAR PROCESSOR

DESCRIPTIVE NOTES *(Type of report and inclusive dates)*
Electrical Engineer's Thesis; December 1972

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REPORT DATE December 1972	7a. TOTAL NO. OF PAGES 151	7b. NO. OF REFS 2

. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
b. PROJECT NO.	
c.	9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*
d.	

0. DISTRIBUTION STATEMENT

Approved for public release; distribution unlimited.

1. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY Naval Postgraduate School Monterey, California 93940

3. ABSTRACT

Bistatic radar is different from conventional (monostatic) radar in that the transmitting and receiving antennas are in separate locatoins. For purposes of this thesis the transmitting radar will be assumed to be located up to 100 miles from the bistatic radar receiver. It will have a circular scan antenna with a constant rotation rate. The plan position indicator (PPI) display of the video from the bistatic radar receiver has both angular and range distortion caused by the wide separation of the transmitting and receiving antennas.

The bistatic radar processor receives video signals from the bistatic receiver and processes them to obtain the information required to synchronize the PPI display's rotation in rate and phase to the rotation of the transmitting antenna and to correct the range errors.

This thesis discusses the design and fabrication of a simplified version of the processor and how it accomplishes the functions mentioned above.

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
BISTATIC RADAR						
RANGE CORRECTION						
RADAR						